# HOT CARRIER DEGRADATION IN DEEP SUBMICRON N-MOS TECHNOLOGIES

A Thesis Submitted to

De Montfort University Leicester

for the Degree of Doctor of Philosophy

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**To My Brother Rajeev**

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# DECLARATION

This thesis contains the results of research undertaken by the author between October 1998 to December 2001 in the Emerging Technologies Research Centre, De Montfort University, Leicester. This research is my own work and contains nothing in collaboration except where explicit acknowledgement is given. This work has not been submitted in whole or in part for any other University degree or diploma.

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# ABSTRACT

With the aggressive scaling of MOS devices hot carrier degradation continues to be a major reliability concern. The LDD technologies, which have been used to minimise the hot carrier damage in MOS devices, suffer from the spacer damage causing the drain series resistance degradation, along with the channel mobility degradation. Therefore, in order to optimise the performance and reliability of these technologies it is necessary to quantify the roles of spacer and channel damages in determining their degradation behaviour. In this thesis the hot carrier degradation behaviour of different generations of graded drain (lightly doped, mildly doped and highly doped) n-MOS technologies, designed for 5V, 3V and 2V operation is investigated. The stress time beginning from microseconds is investigated to study how the damage initiates and evolves over time. A technology dependent two-stage degradation behaviour in the measured transconductance with an early stage deviating from conventionally observed power law behaviour is reported. A methodology based on conventional extraction procedure using the L-array method is first developed to analyse the drain series resistance and the mobility degradation. For 5V technologies the analysis of the damage using this methodology shows a two-stage drain series resistance degradation with early stage lasting about 100ms. However, it is seen that the conventional series resistance and mobility degradation methodology fails to satisfactorily predict degradation behaviour of 3V and 2V technologies, resulting in unphysical decreasing extracted series resistance. It is shown that after the hot carrier stress a change in the universal mobility behaviour for channel lengths approaching quarter micron regime has a significant effect on the parameter extraction. A modified universal mobility model incorporating the effect of the interface charge is developed using the FN stress experiments. A new generalised extraction methodology modelling hot carrier stressed device as series combination of undamaged and damaged channel regions, along with the series source drain resistance is developed, incorporating the modified universal model in the damaged channel region. The new methodology has the advantage of being single device based and serves as an effective tool in evaluating the roles of series resistance and mobility degradations for technology qualification. This is especially true for the deep submicron regime where the conventional extraction procedures are not applicable. Further, the new extraction method has the potential of being integrated into commercial device simulation tools, to accurately analyse the device degradation behaviour in deep submicron regime.

# CHAPTER 1

# INTRODUCTION

## 1.1 Overview

The continued growth in VLSI industry has followed from the ability to shrink the device dimensions enabling faster circuit speed, lower power dissipation and higher packing density. This has been made possible by CMOS "scaling" together with the advances in device manufacturing technology. The most commonly followed scaling rules proposed by Dennard et. al. [1] are based on the "constant field scaling" premise. Under this scheme, both device (active and passive) dimensions and operating voltages are reduced maintaining constant field in both scaled and unscaled devices. However, in practice, due to non-scaling effects associated with threshold voltage, subthreshold swing, depletion layer width and need to have standardised operating voltages (e.g. 5V, 3V, 2V etc.), non-constant field or so called "generalised" scaling has been used [2]. This has resulted in device operating voltages higher than the limit set by constant field scaling and consequently the electric field in the device has gradually increased over successive generation of technologies. This is illustrated in Fig. 1.1, which shows the peak electric field obtained using 2D device simulator MEDICI [3] as a function of operating voltage for different technologies studied in this work (c. f. Table 4.1). In Fig. 1.1 the channel lengths of the corresponding technologies are also shown. The increase of the electric field in the device with scaling, despite the reduction of the operating voltages, highlights the breakdown of constant field scaling and the consequent concern for the hot carrier generation.

As the electric field in the device exceeds the field corresponding to carrier velocity saturation (~4-5x$10^4$V/cm) carrier heating takes place, causing hot carrier generation detrimental to device reliability. The hot carrier degradation in a device results when, under the influence of high electric field in the device, the carriers (electrons and holes) in the channel (largely in the pinchoff) region gain sufficient energy to overcome the barrier between silicon and oxide and get injected into oxide. Once injected into oxide these so-called "hot carriers" create damage in the form of interface states and trapped charge in the oxide layer, which slowly degrade device parameters like threshold voltage, transconductance [4], [5]. This shift in device parameters alters the device characteristics (transfer and output)

and leads to deterioration in the circuit performance causing serious reliability concern. Two basic underlying causes of degradation of device characteristics are: a) shift in the flatband voltage due to presence of the generated charge in the oxide layer, which reflects as shift in the threshold voltage, and b) reduction in the carrier mobility due to the Coulomb scattering by the oxide charge [5]-[6].

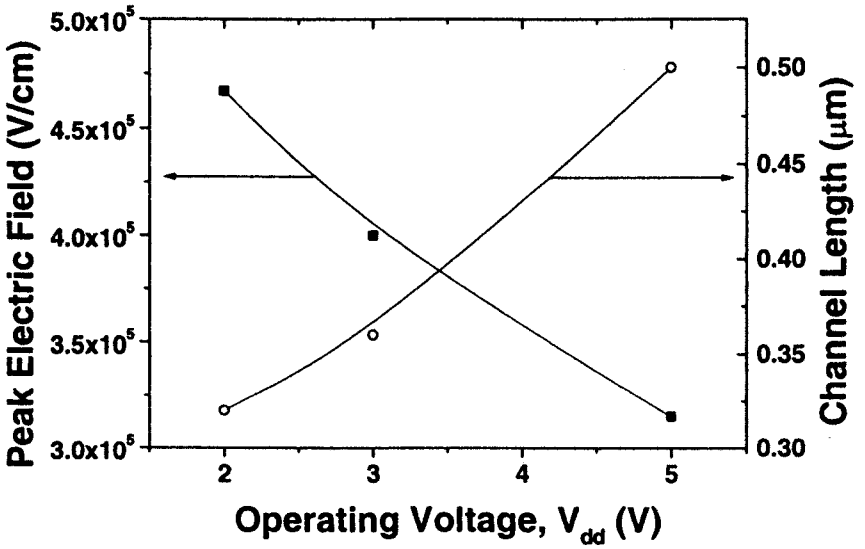


Fig. 1.1 Shows peak electric field and device channel lengths as function of the operating voltage for the technologies studied in this work.

It was recognised in late 1970s that hot carrier degradation can pose limit to device scaling beyond 1μm regime, if the causes leading to their generation are not addressed [7]. Since then the study of hot carrier degradation has became an important issue switching from topic of mere academic concern to an issue affecting the performance and reliability of the state of the art device technologies.

The experimental procedure for the evaluation of the reliability of any device technology is well established after accelerated electrical stress for fairly long times (varying from $10^3$-$10^4$ seconds or more). The degradation in the maximum transconductance or threshold voltage is plotted against time on a log-log scale [4], [5]. This behaviour defined by a power law expression ($At^n$) allows the extraction of device lifetime defined as the stress time corresponding to 5-10% shift in the chosen device parameter. This method has been extensively used in the industry for device reliability prediction. Conventionally, the slope of this plot is also considered to be indicative of the degradation mechanism, with slopes greater

than or equal to 0.5 corresponding to interface state generation and slopes in the range of 0.2-0.3 corresponding to electron trapping [5], [8].

As pointed out above the concern for the hot carrier reliability first became serious when channel lengths were scaled to 1μm regime. It was soon realised that conventional 5V $n^+$ drain technologies could no longer meet hot carrier reliability requirement [9]. This lead to a need for new device designs addressing the limitation posed by hot carriers [10], [11]. Since high electric field in the drain region of a device is the driving force behind hot carrier generation, efforts have been concentrated on reduction of channel electric field in the device so that hot carrier degradation can be kept with in tolerable limits. In this respect the introduction of lightly doped drain (LDD) or graded drain devices in general achieve a major breakthrough in the reduction of hot carrier generation [10]. This approach, often referred to as "drain engineering" relies on spreading the voltage dropped in the pinchoff region over wider region extending into the drain thus reducing the electric field by using low drain doping in the drain drift region instead of conventional $n^+$ drain doping profile. In addition the specially tailored drain engineering profiles also allow the control of the location of the hot carrier generation to minimise the hot carrier injections into oxide layer [12], [13].

With aggressive scaling of CMOS technologies, the challenges on process design are becoming increasingly complex. High-speed technologies require immunity from short channel effects, thinner gate dielectrics, higher channel doping and optimum drain engineered structures with high immunity to hot carrier damage. In this contest, MOSFET scaling with conventional LDD structure is also fast approaching its performance limits. This is because of serious limitations placed on the increasing parasitic source/drain series resistance from shallow LDD regions, which reduces the maximum drive capability. Further, during optimisation of an LDD structure, any increase in doping causes a conflict due to the accompanying increase in the peak electric field and thereby hot carrier related damage. Process development of sub-half micron technologies therefore requires a fine balance to be maintained between the circuit performance and its reliability.

Despite the number of advantages the "drain engineered" technologies offer over conventional devices; they do have some limitations. One of the major drawback of these technologies has been the problem associated with the series resistance increase. The problem arises because of the lack of gate control over current conduction in the spacer region and

consequent increased susceptibility of series resistance to damage in spacer oxide [14]. The conventional long term accelerated ageing lifetime plots discussed above provide little or no information as to the specific roles of various process parameters such as spacer geometry and implantation dose, energy or angle on the hot carrier degradation behaviour. Furthermore, accurate dependence of the circuit performance itself on these process variations also becomes increasingly complex because of difficulties associated with extraction of MOSFET parameters at small gate geometries and the validity of conventional equations to describe the MOS I-V characteristics after hot carrier stress. This has led to need for developing new methods of characterisation and study the hot carrier degradation of LDD devices. In the past decade lot of effort has been devoted to understanding the degradation behaviour of LDD MOSFETs [14]-[19]. These studies have focussed on the time evolution of degradation behaviour of these technologies, their impact on conventional lifetime prediction and mechanism of degradation in LDD technologies.

## 1.2 Motivation and Objectives

The studies have shown that degradation of LDD technologies show markedly different behaviour than observed for the conventional technologies [15], [16], [18], [19]. It has been reported that degradation in these technologies show two stage saturating behaviour [15]. This has been explained on the basis of increase in drain series resistance due to damage in spacer region, along with the damage in channel region causing mobility degradation as in conventional technologies. The saturating nature of degradation is attributed to saturating nature of the damage in spacer region. The study of series resistance degradation using conventional extraction methods based on devices of different channel lengths belonging to the same technology, the so called "L-Array" method, [20], [21] have indeed confirmed this conclusion [17], [18], [22].

The majority of the work in the literature has focussed on generation of LDD technologies in 0.5-1μm regime, mostly 5V as standard operating voltage [15]-[19]. But as the technologies are scaled to sub-half micron regime, the operating voltages have to be reduced from 5V standard to 3V, 2V and lower to meet the hot carrier reliability requirements and more complex drain engineered structures have been implemented [12], [13]. There are two main issues where current knowledge and understanding of degradation behaviour in these technologies is limited:

1. Although the long term d. c. hot carrier degradation of LDD MOSFETs has been widely reported, there is a significant lack of knowledge about the d. c. degradation behaviour for short stress time scales (early stage). Studying early stage degradation behaviour is important since under normal operation it is likely that the device will suffer from this type of damage within very short span of operation thus affecting its lifetime. Further for LDD MOSFETs, understanding the mechanisms of hot carrier degradation in the oxide spacer region of LDD MOSFETs is an important aspect of device reliability and process design.

2. In the design of any LDD technology the hot carrier performance is a fine balance between series resistance increase due to damage in the spacer region and channel mobility decrease due to damage in the channel region [14]. Thus for a particular technology roles of spacer and channel damage need to be quantitatively accessed. There have been studies reported in the literature to quantify these roles [5], [17], [18], [22], [23] using series resistance and mobility extraction methods. But these techniques have limited application in studying channel and spacer degradation behaviours in deep sub-micron regime as these techniques: a) do not fully consider the effect of channel damage on mobility behaviour and b) the effect of scaling on degradation behaviour of device parameters like threshold voltage. These limitations have pronounced effect on characterisation of spacer and channel degradation through series resistance and mobility degradation in sub-half micron regime. Thus there is a need for a new approach for quantifying roles of channel and spacer damages in these technologies along with the need for understanding the effect of scaling on degradation behaviour associated with series resistance and channel mobility.

In this thesis, problems relating to spacer and channel damages highlighted above in different technology generations are studied. The main objectives of this work are:

1. To study the evolution of degradation behaviour LDD technologies with stress time scales beginning from microseconds

2. To identify the roles of spacer and channel damages in determining the degradation behaviour.

3. A study of the mechanisms of spacer degradation.

4. To develop a consistent methodology for the separation of spacer and channel degradations using series resistance and mobility extraction and study the impact of scaling on channel and spacer degradation behaviour.

## 1.3 Major Outcomes of this Work

1. A new early stage hot carrier degradation behaviour of graded drain n-MOS technologies, showing deviation from conventional power law behaviour is reported. It is seen that, compared to the single power law degradation widely reported in the literature, the hot carrier degradation in these technologies progresses in two stages with an early stage dominated by the damage in the spacer region, leading drain series resistance increase.

2. The problem of drain series resistance and channel mobility degradation caused by hot carrier stress is extensively studied. It is shown that extraction of series resistance and mobility degradation based on the conventional extraction method has a limited application to the cases where hot carrier damage in the device is small, as is the case long channel devices.

3. A modified universal mobility model considering effect of interface charge on model parameters is developed. It is shown that for channel lengths in quarter micron regime the channel damage leads to a deviation in the universal mobility behaviour, which is not taken into account in the conventional extraction methods.

4. A new generalised extraction methodology for drain series and mobility degradation is developed in this work, which overcomes shortcomings of the exiting methods. This methodology is a more accurate treatment of the hot carrier damage device considering separate models for damaged and undamaged regions. It incorporates the deviation in the universal model in the localised region of the hot carrier damage and successfully addresses the problems associated exiting methods.

## 1.4 Organisation of this Thesis

Chapter 2 reviews basic operational principles of MOS devices. The current conduction models for the device under different regions of operation are presented. A discussion of short channel effects like effective mobility, velocity saturation on device equations is then presented.

Chapter 3 reviews hot carrier degradation mechanisms in n-MOS devices. The hot carrier generation and device degradation are first presented, followed by a review of lifetime prediction methodologies. The need for lightly doped drains is discussed, highlighting the benefits of these technologies in reducing hot carrier generation and lifetime improvements. The disadvantages of the lightly drain technologies are discussed further, stressing the need for characterisation of different degradation mechanisms associated with these technologies in deep submicron regime.

Chapter 4 of this thesis covers the experimental techniques used in this work to stress and characterise both the short and long term degradation behaviours. The different characterisation methods used to analyse the degradation behaviour are also presented. The structural details of device technologies used in the study are also given in this Chapter.

Chapter 5 presents experimental results of degradation behaviour of the 5V, 3V and 2V technologies. It demonstrates existence of device dependent early stage degradation behaviour. A qualitative model to explain degradation behaviour based on damage in spacer region and channel region is presented.

Chapter 6 focuses on detailed analysis of degradation behaviour of 5V technologies. A methodology to extract the degradation of drain series resistance and mobility is first developed and then applied to the degradation behaviour of these technologies. The results clearly distinguish the degradation of series resistance associated with the spacer damage and various stages of the damage in the spacer region. The nature of the damage in the spacer region is analysed by alternate stress experiments and charge pumping measurements. The causes of saturating behaviour of spacer degradation are discussed in the end.

In Chapter 7 the failure of conventional series resistance and mobility extraction methodology (developed in Chapter 6) for extraction of parameter degradation behaviour in 3V and 2V technologies is demonstrated. It is seen that for channel length approaching quarter-micron regime as result of nonscaling nature of the hot carrier damage in the channel region leads to the deviation in universal mobility model. Thus, the universal model assumed to be constant in the conventional extraction methodology is no longer valid after hot carrier stress at very short channel lengths. This highlights the need to take into account the effect of damage in the channel region on the universal mobility.

Chapter 8 is devoted to the development of a modified universal model to take into consideration the effect of the interface charge on universal mobility parameters. The FN stress experiments are used to eliminate any spacer-related damage and study the effect of interface charge on universal mobility behaviour.

Chapter 9 presents a new generalised extraction methodology for parameter extraction after hot carrier stress. This methodology takes into account the modified universal mobility model developed in Chapter 8 and successfully addresses the problems encountered with conventional extraction procedure of Chapter 6. The new methodology is validated both by good fit between calculated and extracted parameters like transconductance, threshold voltage and consistent degradation behaviour obtained for different technologies.

Chapter 10 summarises major outcomes of this study along with the suggestion future the work.

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# CHAPTER 2

# MOS DEVICE PHYSICS

## 2.1 Introduction

Metal-Oxide-Semiconductor (MOS) structure lies at the heart of CMOS technology. The VLSI technology owes its success to the excellent qualities of silicon dioxide ($SiO_2$) and its interface with silicon, which is indispensable for the field effect control of surface conductivity. The Si-$SiO_2$ system and the operation of MOS based devices have been extensively treated in [1]-[4]. In this Chapter, the fundamental properties of the MOS system and its basic operational principles, necessary for understanding of hot carrier phenomena and their effects on device characteristics are reviewed. The system of equations, describing both MOS capacitor and MOS transistor under different regions of operation, are described.

## 2.2 MOS Capacitor

The MOS structure, shown in Fig. 2.1, consists of a Silicon substrate (p or n type), a thermally grown oxide of thickness $t_{ox}$ and a gate electrode (metal or heavily doped polysilicon). The energy band diagram for the ideal system, when metal and semiconductor work functions are equal, is shown in Fig. 2.2. The equality of metal semiconductor work functions implies that

$$\Phi_M = \chi + E_g/2 + q\phi_B \tag{2.1}$$

where $\Phi_M$ is the metal work function, $\chi$ is the semiconductor electron affinity, $E_g$ is the Silicon band gap and $\phi_B$ is the Fermi potential defined as difference between the Fermi level $E_f$ and the intrinsic energy level $E_i$. Since, metal and semiconductor work functions are equal in this case, the metal and semiconductor Fermi levels line up and the energy bands in semiconductor and oxide are flat. This is known as the flatband condition. The equilibrium carrier concentrations in the Si remain unchanged in this case and are given in [1]

$$n = n_i e^{(E_f - E_i)/kT} \tag{2.2}$$

$$p = n_i e^{(E_i - E_f)/kT} \tag{2.3}$$

where n and p are free electron and hole concentrations in the substrate respectively and $n_i$ is the intrinsic carrier concentration in undoped Silicon.

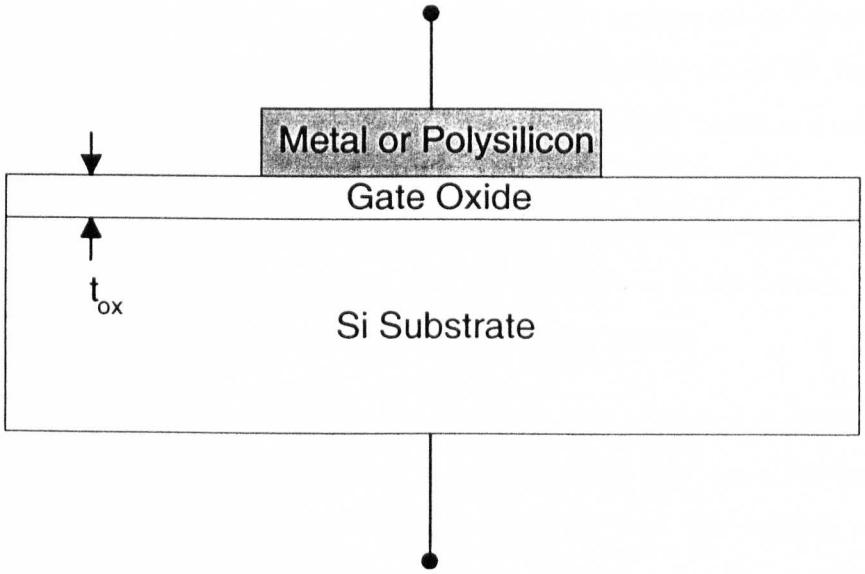


Fig. 2.1 MOS Capacitor.

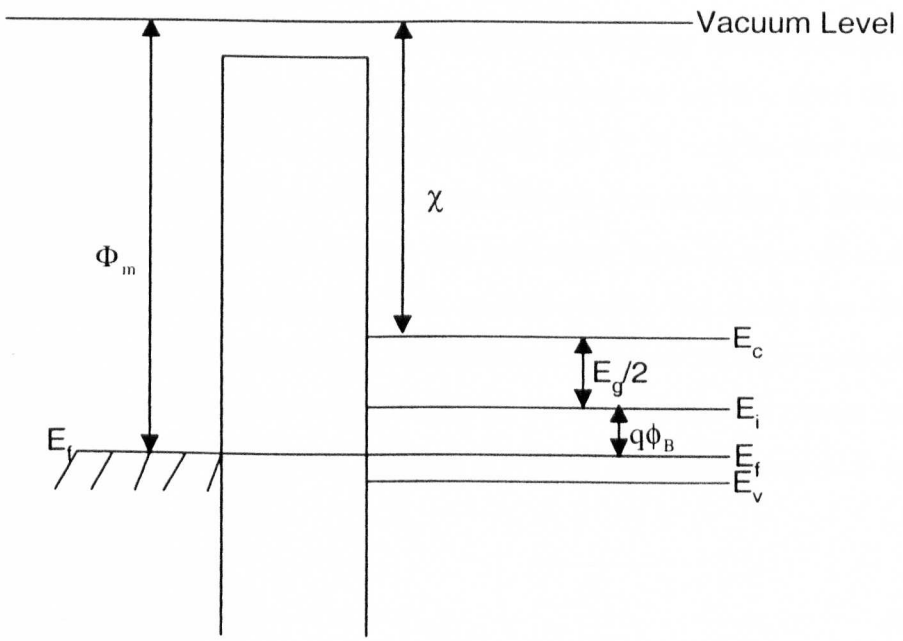


Fig. 2.2 Flatband condition when the metal and semiconductor work functions are equal.

### 2.2.1 Accumulation, Depletion and Inversion

The energy band diagram for the MOS system when a negative voltage is applied to the gate electrode is shown in Fig. 2.3. The metal Fermi level is raised with respect to the semiconductor Fermi level by the applied gate voltage. This induces electric field in the gate oxide in a direction that attracts hole towards the Si-$SiO_2$ interface. Since the Fermi level in the absence of any current conduction remains constant, all other bands are raised upward near the surface due to induced electric field in Si. As a result the intrinsic level $E_i$ at the surface moves away from the Fermi level than in the bulk Si. This according to (2.3) leads to hole concentration at surface much higher than the equilibrium concentration. This excess holes accumulation at the surface is called as accumulation condition.

If positive voltage is applied to the gate metal the Fermi level is pushed downward as shown in Fig. 2.4. This causes field in the oxide and in the Si substrate that pushes the holes near the Si surface into bulk leaving behind uncompensated acceptor ions. The intrinsic energy level in this case is pushed downward closer to Fermi level which according to (2.2) results in lower hole concentration near the surface than in the bulk. Since the holes are depleted from surface this is called depletion condition.

As $V_g$ is further increased the energy levels near the Si surface are further pushed downward as a result of the increased field such that at the Si surface the intrinsic level ($E_i$) becomes lower than Fermi level ($E_f$). This, according to (2.2) and (2.3), implies that nearly all the holes are depleted from surface and free electron concentration at surface is greater than the bulk concentration is induced at the surface. For sufficiently large $V_g$ when $E_i$ at the surface lies as far below $E_f$ as it is above $E_f$ in the bulk, as shown in Fig. 2.5. Under this condition the surface electron concentration is equal to bulk hole concentration. As carrier concentration at the surface is equal to but opposite in polarity to that of the substrate, it is known as inversion condition. At this condition the surface potential defined as difference between $E_i$ in bulk and $E_i$ at surface is given in [1], [2]

$$\psi_s(\text{inv.}) = 2\phi_B = 2\frac{kT}{q}\ln\frac{N_B}{n_i} \qquad (2.4)$$

where $N_B$ is substrate doping. Using (2.3) surface electron concentration can be expressed as [1], [2]

$$n = \frac{n_i^2}{N_B} e^{q\psi_s / kT} \tag{2.5}$$

Thus, under inversion condition, the electron surface concentration varies exponentially with the surface potential and under strong inversion condition surface electron concentration two to three orders of magnitude higher than substrate hole concentration can be obtained.

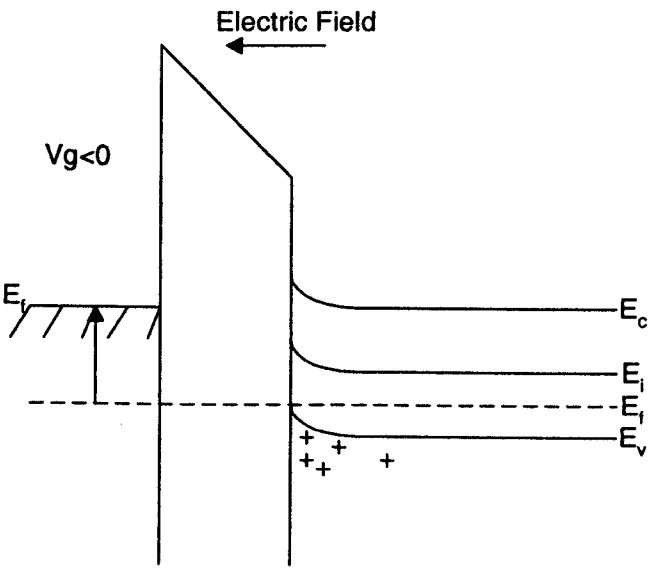


Fig. 2.3 Energy band diagram under accumulation.

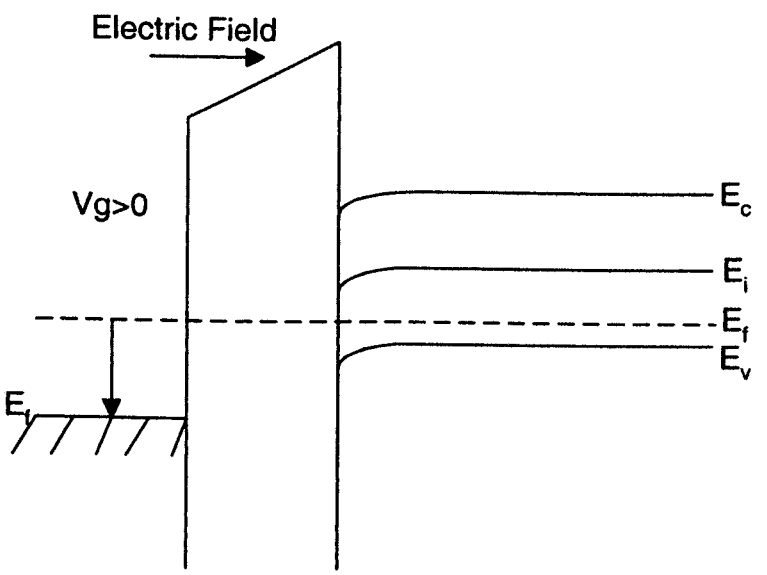


Fig. 2.4 Energy band diagram under depletion.

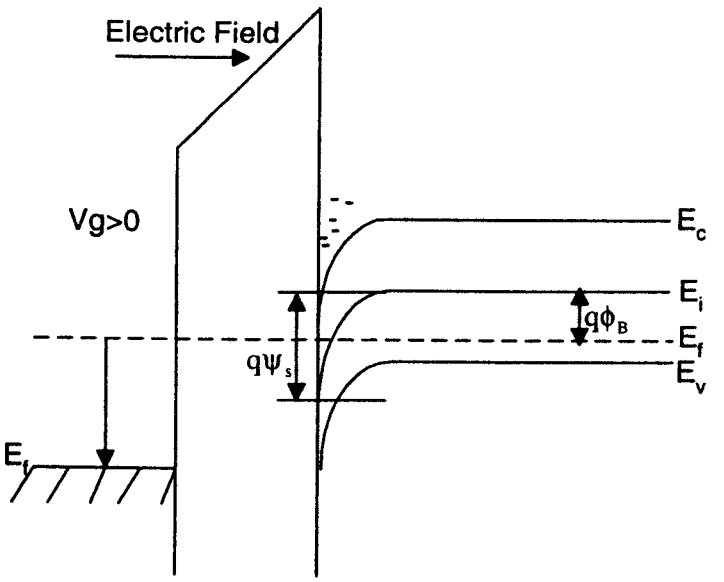


Fig. 2.5 Energy band diagram under inversion.

### 2.2.2 Threshold Voltage

In the absence of any oxide charge and zero metal semiconductor work function difference the total charge per unit area placed on the gate is equal to total charge per unit area, $Q_s$, induced in Si. In terms of potential distribution across MOS device the applied gate voltage, $V_{gs}$, appears as voltage across oxide, $V_{ox}$, and voltage induced in Si, $\psi_s$, due to band bending. This can be expressed as [2], [3]

$$V_{gs} = V_{ox} + \psi_s = -Q_s / C_{ox} + \psi_s \tag{2.6}$$

where $C_{ox}$ is the oxide capacitance per unit area given by $\varepsilon_{ox}/t_{ox}$. At the onset of inversion, $Q_s$ can be approximated by depletion charge per unit area, $Q_d$, due to ionised acceptors, which is given by [2], [3]

$$Q_d = -qN_B W_d = -(2q\varepsilon_{Si} N_B \psi_s)^{1/2} \tag{2.7}$$

where $W_d$ is depletion layer width. Using (2.4), (2.6) and (2.7) threshold voltage, $V_t$, is obtained by setting $\psi_s = 2\phi_B$ at the onset of inversion

$$V_t = 2\phi_B + \frac{(4\varepsilon_{Si} q N_A \phi_B)^{1/2}}{C_{ox}} \tag{2.8}$$

Eq. (2.8) is the expression for threshold voltage in ideal case. In actual cases, however, the metal semiconductor work function difference ($\Phi_{MS}$) is nonzero and charge in the form of fixed oxide charge, interface states etc. is present in the oxide. This charge can be expressed as an equivalent charge ($Q_{ox}$). As a result of finite $\Phi_{MS}$ and $Q_{ox}$ the bands the Si and oxide are no longer flat at zero gate bias. In order to compensate for additional charge induced due to metal semiconductor work function difference and oxide charge, an additional voltage of amount $V_{FB}$ is needed to be applied at the gate to achieve flat band condition

$$V_{FB} = \Phi_{MS} - Q_{ox} / C_{ox} \tag{2.9}$$

The threshold voltage as result of (2.9) modifies to

$$V_t = V_{FB} + 2\phi_B + \frac{(4\varepsilon_{Si} q N_A \phi_B)^{1/2}}{C_{ox}} \tag{2.10}$$

## 2.3 The MOS Transistor (MOSFET)

The metal oxide semiconductor field effect transistor (MOSFET) is the building block of modern VLSI circuits and dynamic memories. Because carriers of one polarity (e. g. electrons or holes) carry the current in the device, these devices are also referred to as unipolar or majority carrier devices. The basic structure of an n-channel MOSFET is shown in Fig. 2.6. It is a four terminal device with source, drain, gate and substrate terminals. The source and drain terminals are $n^+$ regions formed by ion implantation, the substrate is p type usually epitaxial layer and the gate is either metal or heavily doped poly-silicon. The gate is separated from substrate by insulating layer normally silicon dioxide ($SiO_2$) called the gate oxide. The surface region between source and drain is called channel, this region is critical for the operation of MOSFET. The effects of the gate voltage on channel conductivity are similar to that of two-terminal MOS described in the previous sections and concepts of accumulation and inversion can be directly applied to MOSFET operation.

### 2.3.1 Drain Current

The conduction between source and drain terminal of MOSFET shown in Fig. 2.6 can be controlled by application of gate voltage $V_{gs}$. When the gate voltage is lower than critical voltage called threshold voltage $V_t$ the MOSFET current is dominated by diffusion current

between source and drain terminals and because of its small magnitude the transistor is said to be in the 'off' state.

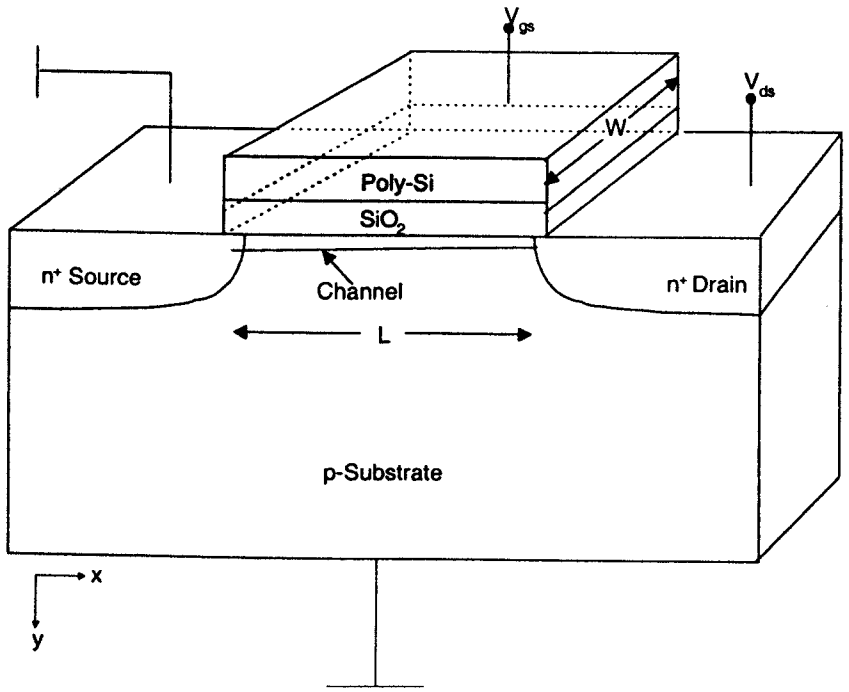


Fig. 2.6 Three-dimensional view of n-channel MOSFET structure.

When the gate voltage is larger than $V_t$ an n-type inversion layer is formed in the channel region and the current is dominated by drift component and the transistor is said to operate in 'on' state. The current density at any point (x, y) along the channel is given by [2], [3]

$$J_n(x,y) = -q\mu_n n(x,y)\frac{dV(x)}{dx} \qquad (2.11)$$

where $J_n$ (x,y) is the current density, q electron charge, $\mu_n$ is the electron mobility n(x,y) is electron density and V(x) is the channel potential. The total drain current at any point along the channel ($I_{ds}$) can be obtained multiplying (2.11) with the width W of the device and integrating over x from y=0 to y=$y_i$

$$I_d(x) = qW\int_0^{y_i}\mu_n n(x,y)\frac{dV(x)}{dy}dy\,. \qquad (2.12)$$

where $y_i$ is the thickness of the inversion layer. For the development of one dimension model a gradual channel approximation (GCA) is used which assumes that variation of electric field in x direction (along the channel) is much less than the corresponding variation in the y direction (perpendicular to the channel). This means that the term dV(x)/dy in (2.12) can be taken outside the integral. Further by defining effective mobility $\mu_{n,eff}$ as [3]

$$\mu_{n,eff} = \frac{\int_0^{y_i} \mu_n n(x,y)dy}{\int_0^{y_i} n(x,y)dy} \tag{2.13}$$

Using (2.13), $I_{ds}(x)$ can written as

$$I_{ds}(x) = -\mu_{eff} W \frac{dV}{dx} Q_i(x) \tag{2.14}$$

where $Q_i(x) = q\int_0^{y_i} n(x,y)dy$. Integrating (2.14) over channel length gives the total drain current

$$I_{ds} = -\mu_{eff} \frac{W}{L} \int_0^L Q_i(x)dV \tag{2.15}$$

### 2.3.2 Charge Sheet Model

In order to determine an analytic expression for the drain current as a function of terminal voltages, a charge sheet model of the inversion layer is used. In this model the inversion layer is treated as sheet of charge of negligible thickness in which both inversion layer and depletion layer charge are controlled by the gate voltage. At the onset of inversion the surface potential is given in [2], [3]

$$\psi_s = 2\phi_B + V(x) \tag{2.16}$$

where V(x) is the channel potential at any point x in the channel due to the applied drain voltage $V_{ds}$. As a result of the varying V(x) the depletion layer charge density and total silicon charge density also vary along the channel and are given in [2], [3]

$$Q_d = qN_A W_m = [2\varepsilon_{si} qN_A (2\phi_B + V(x))]^{1/2} \quad (2.17)$$

$$Q_s(y) = -C_{ox}(V_{gs} - V_{FB} - 2\phi_B - V(x)) \quad (2.18)$$

The inversion layer charge density is given by the difference between silicon and depletion layer charge densities and is given by

$$Q_i(y) = -C_{ox}(V_{gs} - V_{FB} - 2\phi_B - V(x)) + [2\varepsilon_{si} qN_A (2\phi_B + V(x))]^{1/2} \quad (2.19)$$

Substituting (2.19) into (2.15) and carrying out the integration, drain current can be expressed as

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L}\left[(V_{gs} - V_{FB} - 2\phi_B - \frac{V_{ds}}{2})V_{ds} - m[(2\phi_B + V_{ds})^{3/2} - (2\phi_B)^{3/2}]\right] \quad (2.20)$$

where m is a constant given by $m = \frac{2(2\varepsilon_{Si} qN_A)^{1/2}}{3C_{ox}}$, with $\varepsilon_{si}$ as dielectric constant of Si.

Eq. 2.20 is the generalised drain current model for device current. In particular two cases of (2.20), which are of interest, are considered below.

### 2.3.3 Linear Region

When $V_{ds}$ is small the second term in (2.20) can be expanded in power series in $V_{ds}$ keeping first order terms gives drain current in linear region [3]

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L}\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds} \quad (2.21)$$

where $V_t$ is threshold voltage given by

$$V_t = V_{FB} + 2\phi_B + \frac{(4\varepsilon_{Si} qN_A \phi_B)^{1/2}}{C_{ox}} \quad (2.22)$$

In this region of operation the current varies linearly with the gate voltage. This expression is most commonly used to extract the device threshold voltage by linear extrapolation of the measured $I_{ds}$-$V_{gs}$ characteristics.

### 2.3.4 Saturation Region

At large drain voltages higher order terms in (2.20) also become important and keeping second order terms in power series expansion of (2.20) the drain current becomes

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L}\left( V_{gs} - V_t - \frac{\gamma}{2} V_{ds} \right) V_{ds} \tag{2.23}$$

where

$$\gamma = 1 + \frac{(\varepsilon_{Si} q N_A / 4\phi_B)^{1/2}}{C_{ox}} \tag{2.24}$$

is the body effect coefficient and represent the effect of substrate bias on threshold voltage and drain characteristics. When drain bias is increased, the surface potential at drain end increases according to (2.16) and the inversion layer charge density decreases according to (2.19) until a until a point at which it becomes zero. At this point the drain current saturates and is referred to pinch off point. The drain voltage at pinch off is called as $V_{dsat}$ and is determined by setting (2.19) to zero at drain end i.e. $Q_i(L)=0$

$$V_{dsat} = \frac{(V_{gs} - V_t)}{\gamma} \tag{2.25}$$

The saturation drain current can be determined by letting (2.25) in (2.23) [3]

$$I_{dsat} = \mu_{eff} C_{ox} \frac{W}{2\gamma L} (V_{gs} - V_t)^2 \tag{2.26}$$

This is also known as square law region since drain current varies as square of the gate voltage. The operation of MOSFET under high drain voltages in saturation is responsible for generation of variety of hot carrier effects, which is discussed in detail in the following Chapter 3.

### 2.3.5 MOSFET Channel Mobility

It has been well known that due to additional scattering mechanisms the carrier mobility in the inversion layer is lower than the bulk mobility. These mechanisms include surface phonon, and surface roughness scattering, which results from movement of carriers confined to inversion layer near Si-$SiO_2$ [5]. When effective mobility is plotted as a function of the

gate voltage it increases first and peaks around threshold voltage, and then falls monotonically as gate voltage is further increased. A widely used first order empirical model describing this dependence is [4]

$$\mu_{eff} = \frac{\mu}{1+\theta(V_{gs} - V_t - V_{ds}/2)} \tag{2.27}$$

where $\theta$ is a parameter describing the effect of vertical field on carrier mobility.

In a work reported by Sabnis and Clements [6] it was shown that effective mobility defined by (2.13) has a universal dependence on effective normal field perpendicular to the interface, independent of substrate bias, substrate doping and the gate oxide thickness. The effective normal field is defined as average field experienced by inversion layer carriers and is defined as [2]

$$E_{eff} = \frac{Q_d + Q_i/2}{\varepsilon_{Si}} \tag{2.28}$$

where $Q_d$ is inversion layer charge at the onset on inversion and $Q_i$ is the inversion layer charge given by [3]

$$Q_d = (4\varepsilon_{Si} q N_A \phi_B)^{1/2} \approx C_{ox}\left(V_t - \frac{V_{ds}}{2}\right) \tag{2.29}$$

$$Q_i \approx C_{ox}\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right) \tag{2.30}$$

Using (2.29) and (2.30), (2.28) can be expressed as

$$E_{eff} = (V_{gs} + V_t)/6t_{ox} \tag{2.31}$$

Recently it has been reported that for thin oxides the empirical universal mobility model follows a more generalised relation given by [7]

$$\mu_{eff} = \frac{\mu}{1+(E_{eff}/E_c)^{\gamma}} \tag{2.32}$$

where $E_c$ and $\gamma$ are model parameters. Using (2.31), (2.32) universal model can be expressed as a function terminal voltages as [7]

$$\mu_{eff} = \frac{\mu}{1+\theta(V_{gs}+V_t-V_{ds}/2)^{\gamma}} \tag{2.33}$$

where parameter $\theta$ depends on oxide thickness and substrate doping and its value are different to that in (2.27).

### 2.3.6 Velocity Saturation

At low lateral field, the carrier velocity field relationship is linear. But as the channel length is reduced, the lateral electric field increases and carrier velocity deviates from linearity. Therefore in order to correctly obtain drain current, the lateral electric field dependence of channel mobility need to be considered. The velocity field relation is normally modelled by piecewise linear function defined by [8]

$$v = \frac{\mu_{eff}E}{1+(E/E_{sat})} \qquad E < E_{sat} \tag{2.34}$$

$$v = v_{sat} \qquad E \geq E_{sat} \tag{2.35}$$

where E is lateral electric field, $v_{sat}$ is the carrier saturation velocity and $E_{sat}=2v_{sat}/\mu_{eff}$ is the saturation electric field which has typical value of $2\text{-}4\text{x}10^4$V/cm [3]. The saturation velocities for electrons and holes in MOSFETs are $v_{sat}$~$7\text{-}8\text{x}10^6$cm/s and $6\text{-}7\text{x}10^6$cm/s respectively [8]. Taking the effect of lateral electric field, the expression for drain current (2.23) modifies to

$$I_{ds} = \mu_{eff}C_{ox}\frac{W}{L}\frac{1}{1+(V_{ds}/E_{sat}L)}(V_{gs}-V_t-\frac{\gamma}{2}V_{ds})V_{ds} \tag{2.36}$$

The velocity saturation limited drain current has much lower value than the corresponding long channel model (2.26). The drain voltage at which velocity saturation occurs is given by [9]

$$V_{dsat} = \frac{E_{sat}L(V_{gs}-V_t)}{(V_{gs}-V_t)+E_{sat}L} \tag{2.37}$$

The drain current under velocity saturation can be found from product of carrier density at drain and saturation drift velocity at drain [8]

$$I_{dsat} = v_{sat} W C_{ox} (V_{gs} - V_t - V_{dsat}) \tag{2.38}$$

Letting (2.37) into (2.38) $I_{dsat}$ becomes

$$I_{dsat} = v_{sat} W C_{ox} \frac{(V_{gs} - V_t)^2}{(V_{gs} - V_t) + E_{sat} L} \tag{2.39}$$

For very short channel lengths L→0 (2.39) becomes

$$I_{dsat} = v_{sat} W C_{ox} (V_{gs} - V_t) \tag{2.40}$$

Thus the velocity saturated drain current varies linearly with the gate voltage in contrast to square law model for long channel devices.

### 2.3.7 Subthreshold Region

When the gate voltage is below $V_t$ there exist gradient in electron concentration along the channel. The drain current in this case is dominated by carrier diffusion similar to current conduction in a bipolar transistor. The drain current under this condition can be obtained by considering MOSFET as bipolar device with channel region acting as base [2]

$$I_{ds} = -qAD_n \frac{dn}{dx} = qAD_n \frac{n(0) - n(L)}{L} \tag{2.41}$$

where A is crossectional area for the current flow, $D_n$ is electron diffusion coefficient, n(0) and n(L) are electron densities at source and drain ends. Using (2.5) and (2.16), n(0) and n(L) are given by

$$n(0) = n_0 e^{q\psi_s / kT} \tag{2.42}$$

$$n = n_0 e^{q(\psi_s - V_{ds})/kT} \tag{2.43}$$

Letting (2.42) and (2.43) into (2.41), $I_{ds}$ is given by [2]

$$I_{ds} = \mu_n \frac{W}{2L} \frac{q^2 N_B L_D}{kT} \left( \frac{n_i}{N_B} \right)^2 e^{q\psi_s / kT} (q\psi_s / kT)^{-1/2} \left( 1 - e^{-qV_{ds}/kT} \right) \quad (2.44)$$

where $L_D$ is Debye length given by $L_D=(2kT\varepsilon_{Si}/q^2N_A)^{1/2}$. Since surface potential below threshold is proportional to gate voltage [2], the subthreshold current varies exponentially with the gate voltage. The subthreshold slope given by

$$S = \ln 10 \frac{dV_{gs}}{d(\ln I_{ds})} \quad (2.45)$$

is a useful monitor of determining device on/off switching speed, smaller the value of S better the switching performance. The subthreshold slope depends in general on depletion layer capacitance $C_D$ and capacitance due to interface states density, $D_{it}$ (in $cm^{-2}eV^{-1}$) and are related by [2]

$$S = \ln 10 \frac{kT}{q} \left[ 1 + \frac{C_D}{C_{ox}} + \frac{C_{it}}{C_{ox}} \right] \quad (2.46)$$

where, $C_{it}=qD_{it}$. Knowing $C_{ox}$ and $C_D$, from (2.46), the interface trap distribution can be determined. Although this technique can be used in principle to find interface state and oxide charge densities, it is very sensitive to surface potential variation in the subthreshold region. This results in large fluctuation in calculated values of interface and oxide densities, rendering it very unreliable for detecting small changes in the interface states.

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# CHAPTER 3

# REVIEW OF HOT CARRIER DEGRADATION IN N-MOSFETS

## 3.1 Introduction

The hot carrier degradation of device parameters (transconductance and threshold voltage) for long channel n-MOSFETs were first reported 25 years ago [1]. But the in past two decades the hot carrier degradation has evolved from an academic research topic to a practical issue affecting performance and reliability of state of the art CMOS technologies. The understanding of degradation behaviour in MOS transistor involves understanding the origin of hot carriers generation in the device, their injection mechanism into the insulating layer, the mechanisms and nature of the damage in the insulating layer, and the effect of the damage on device characteristics.

The hot carrier degradation has been reviewed in greater detail in [2]-[4], the purpose of this Chapter is to review the basic hot carrier degradation phenomena in n-MOSFETs to lay the framework for the study presented in the later Chapters. The subject material in this Chapter is fairly hierarchical and chronological in order. It begins by presenting a model for the lateral electric field in the drain saturation region, which is known to be region of majority of hot carrier generation and has been subject of the early studies [5], [6]. The concept of carrier heating in the electric field and treatment of channel electrons as hot electron gas is then discussed briefly [7]. The hot carrier generation, injection and resulting localised damage in the drain region is then discussed [8]-[10]. The effect of the damage on device characteristics is presented defining lifetime and approaches for lifetime prediction are reviewed [8], [11]. The need for lightly doped drains devices as channel lengths are scaled is discussed and their advantages and disadvantages are presented [12]-[14]. This is followed by an outlining of the new drain engineered device designs to overcome the problems associated with conventional LDD devices in deep submicron regime [2], [15].

## 3.2 Electric Field in Velocity Saturated Region

It has been well established that hot carrier generation in MOSFETs is related to the high electric field in the velocity saturated pinch-off region [6]. According to long channel length drain current model discussed in Chapter 2, when the drain voltage is increased such that

channel at the drain end ceases to exist. The drain current becomes independent of the drain voltage and is given by (2.26),

$$I_{dsat} = \mu_{eff} C_{ox} \frac{W}{2\gamma L}(V_{gs} - V_t)^2 \tag{3.1}$$

Under this condition, the channel is said to "pinch off" as shown in Fig. 3.1. The drain voltage when saturation occurs is called saturation voltage ($V_{dsat}$) and is given by (2.37). In this model, since inversion charge density is assumed to be zero at pinch off point, the electric field at this point has to become infinite in order to maintain current continuity. This is obviously an unphysical situation and results from breakdown of gradual channel approximation used in driving long channel drain current model.

In practice the electric field remains finite and becomes comparable to vertical field at pinch off point. So, the control of the vertical field over the inversion layer charge is reduced as the carriers move from the pinch off point toward the drain and as a result the carriers start to leave the surface channel and inject into pinchoff region. The voltage at pinch off point remains constant at $V_{dsat}$ and the difference $V_{ds}$-$V_{dsat}$ is dropped across the depletion region between pinch off point and the drain. The length of this region marked as $\Delta L$ in Fig. 3.1 increase as $V_{ds}$ is increased because pinch off point moves towards source with increased lateral field. The carriers injected from channel into this region are velocity saturated, hence this region is called velocity saturation region.

In order to correctly model velocity-saturated region both Poisson's and current continuity equations need to be solved simultaneously for the channel potential and electric field. The approximate solutions for these quantities were given by El Mansy et. al. [5] and improved by Ko. et. al. [6]. In these approaches the solutions for channel potential V(x), the lateral electric field E(x) and $\Delta L$ in velocity saturated region are obtained by simultaneously solving 2D Poisson's and current continuity equations considering appropriate boundary conditions. The solutions for these quantities for a rectangular drain junction are given in [6]

$$E(x) = E_{sat} \cosh(x/l) \tag{3.2}$$

$$V(x) = V_{dsat} + lE_{sat} \sinh(x/l) \tag{3.3}$$

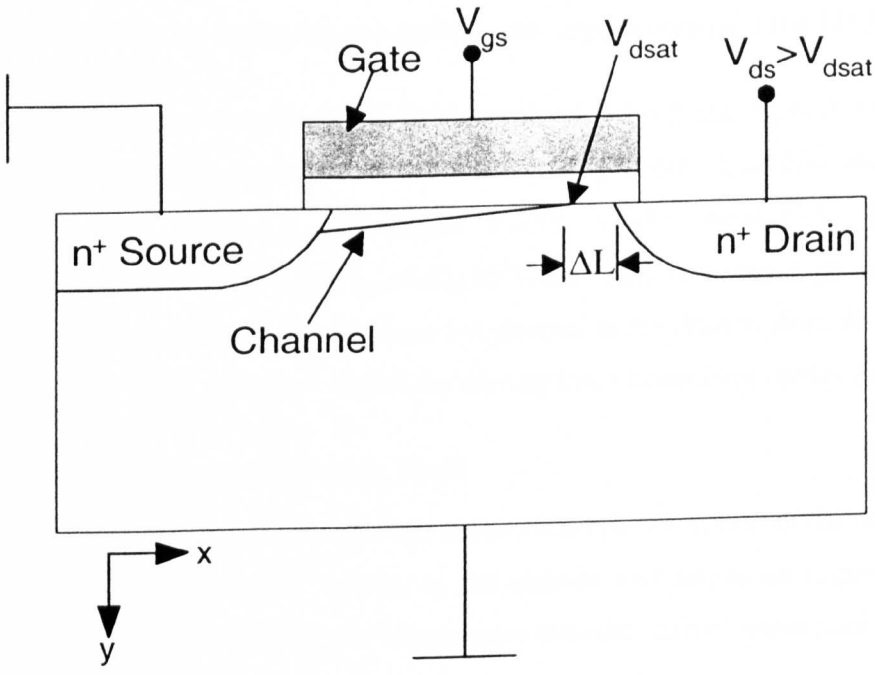


Fig. 3.1 Schematic diagram of n-MOSFET operating in saturation.

$$\Delta L = l \ln\left[\frac{(V_d - V_{dsat})/l + E_m}{E_{sat}}\right] \tag{3.4}$$

where l is characteristic length, $V_{dsat}$ is the saturation drain voltage and $E_m$ is the peak lateral electric field and are given by [7], [8]

$$l \sim 0.22 x_j^{1/2} t_{ox}^{1/3} \tag{3.5}$$

$$V_{dsat} = \frac{E_{sat} L (V_{gs} - V_t)}{(V_{gs} - V_t) + E_{sat} L} \tag{3.6}$$

$$E_m = \left[\frac{(V_d - V_{dsat})^2}{l^2} + E_{sat}^{\ 2}\right]^{1/2} \sim \frac{V_d - V_{dsat}}{l} \tag{3.7}$$

where $x_j$ and $t_{ox}$ are the drain junction depth and oxide thickness respectively. Eqs. (3.2)-(3.7) are fundamental to understanding of generation of hot carriers in velocity saturation region. According to (3.2) the lateral electric field in the saturation region increases almost exponentially towards the drain. This field can become large to cause the generation of

secondary electron hole pairs, which can gain sufficient energy to inject into oxide or cause damage at the oxide by impinging at interface with large energy [8]-[10], [16].

To get a feel of the magnitude of field involved, letting the typical values of device parameters for 5V technologies studied in this work: $x_j$=0.3μm, $t_{ox}$=120Å and L=0.5μm. For a device operated under $I_{submax}$ condition $V_g$=3V, $V_d$=7V, from (3.5), (3.6) and (3.7), $V_{dsat}$=1.08V, l=1.28x10$^{-5}$cm$^{-1}$ and $E_m$=4.58x10$^5$V/cm! This is a very high electric field and causes large impact ionisation to generate hot carriers in the drain region, demonstrating that the electric field in the saturation region the driving force behind hot carrier generation.

## 3.3 Carrier Heating in Electric Field

The hot carrier generation can also be understood from the viewpoint of the concept of carrier temperature. In this model the carriers in the channel and saturation region are treated as heated electron gas with much higher temperature than the lattice temperature [7], [17], [18].

According to this model the carrier heating occurs when the electric field in the channel exceeds velocity saturation [17], [18]. The generation of hot carriers can then be understood from energy exchange between the carriers and the lattice. The carriers in the channel of a MOSFET exchange energy with lattice by phonons. At low lateral electric field, the net rate of energy exchange is zero and carriers are in thermal equilibrium with lattice. But as the electric field is increased the carriers gain energy from field and loose it to lattice by emitting phonons. As the electric field becomes high the carrier energy increases beyond acoustic phonon energy and exchange of energy between lattice and carriers is limited via optical phonon resulting in lower rate of energy exchange between the carriers and the lattice [17], [18]. The reduced rate of loss of energy means that carriers on the average acquire more energy than the energy lost. This results in effective carrier temperature, which is different from the lattice and can be related to the electric field as [17]

$$T_e = T\left[1+\frac{3\pi}{32}\left(\frac{\mu_0 E}{V_s}\right)^2\right] \qquad (3.8)$$

where E is the electric field, $\mu_0$ is carrier mobility and $V_s$ is the velocity of sound in silicon. For saturation electric field of 1.5KV/cm electron temperature doubles over lattice temperature (already hot) and carrier heating sets in. As the electric field increases further the

average carrier temperature becomes significantly different from that of the lattice temperature. At very high field the energy distribution of carriers can be described by effective temperature [19], [7]

$$T_e = q\lambda E/k = 1.2x10^{-2}E \tag{3.9}$$

where $\lambda$ is electron mean free path and k is Boltzman's constant. For typical the peak electric field of $4.6x10^5$V/cm in the saturation region of MOSFET, $T_e$~5500K! Thus the carriers in the high electric field can acquire temperature an order of magnitude higher than lattice temperature and are thus called "hot carriers". This is also demonstrated by the simulated electric field and carrier temperature of a 5V technology device structure using 2D device simulator MEDICI [20] with energy balance module as shown in Fig. 3.2. It is seen that the carrier temperature and the electric field follow each other very closely demonstrating that the electric field is responsible for heating of the channel electrons. Therefore the entire hot carrier related phenomena in MOS transistors can be analysed keeping the electric field central to the description.

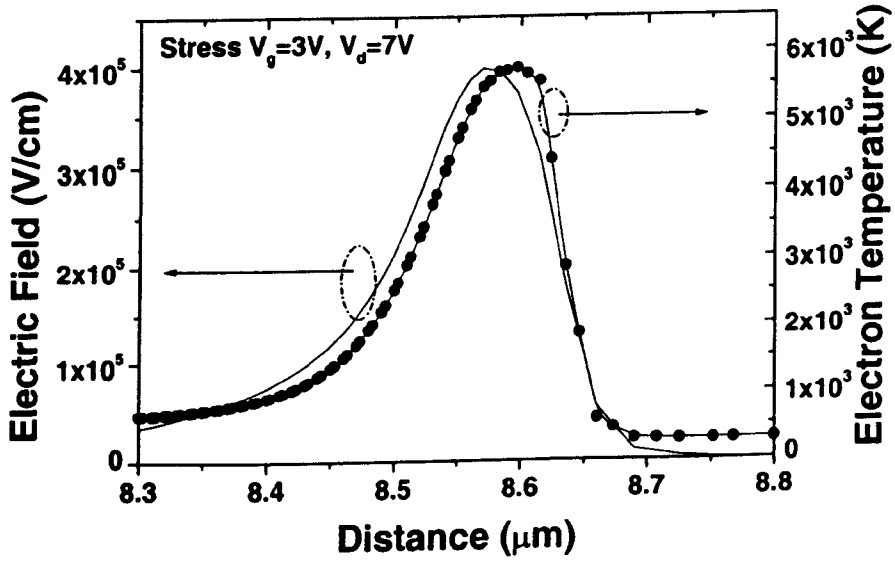


Fig. 3.2 Simulated lateral electric field and carrier temperature profiles for device biased under typical $I_{submax}$ condition: Vg=3V and Vd=7V.

## 3.4 Hot Carrier Generation, Injection into Oxide and Localised Damage

It is pointed out in Sec. 3.3 that whenever the electric field in channel region of a device exceeds saturation electric field severe carrier heating can set in resulting in generation of hot

carriers. This is particularly true for the case of saturation region where a significant fraction of the drain voltage is dropped across region of small length. In saturation mode operation, the electrons leaving the inversion layer are accelerated by the lateral electric field in pinchoff region and gain high energy. When electron energy exceeds the threshold for impact ionisation of about 1.4eV, secondary electron holes pairs are generated. The majority of electrons are collected by the drain terminal while holes are accelerated towards substrate and collected as substrate current.

However some secondary carriers (electrons and/or holes) generated by impact ionisation moving towards Si-$SiO_2$ interface can have energy sufficient to surmount Si-$SiO_2$ barrier (approximately 3.2eV for electrons and 4.3eV for hole injection) and inject into oxide. Such carriers are referred to as the drain avalanche hot carriers (DAHC). The process of impact ionisation, carrier injection into oxide and damage generation is schematically shown in Fig. 3.3. The damage in the oxide occurs in the form of interface states (acceptor/donor type), neutral traps and trapped charge generation [8], [10], [21].

Another types of carriers, which can be injected into oxide, are known as channel hot electrons (CHE). Some channel electrons, which do not suffer energy-loosing collisions in saturation region and have energy larger than barrier height for injection, can undergo redirection towards Si-$SiO_2$ interface and inject into oxide, creating the damage. The end result of the entire hot carrier related injection into oxide is generation of defects, which can acquire charge and affect the device characteristics. Since the high field region is localised near the drain junction the resulting hot carrier injection and damage in the oxide is also localised near the drain junction as illustrated in Fig. 3.3.

### 3.4.1 Substrate Current

The substrate current in n-MOSFET is due to holes generated from impact ionisation by hot carriers as shown in Fig. 3.3. The number of electron hole pairs generated by a carrier per unit length is given by impact ionisation coefficient ($\alpha$)

$$\alpha = \alpha_i e^{-\beta_i / E_m} \tag{3.10}$$

where $\alpha_i$ and $\beta_i$ are parameters whose values for electron induced and hole induced impact ionisation are $2.0\text{x}10^6\text{cm}^{-1}$, $1.7\text{x}10^6\text{cm/V}$ and $8.0\text{x}10^6\text{cm}^{-1}$, $3.7\text{x}10^6\text{cm/V}$ respectively [4].

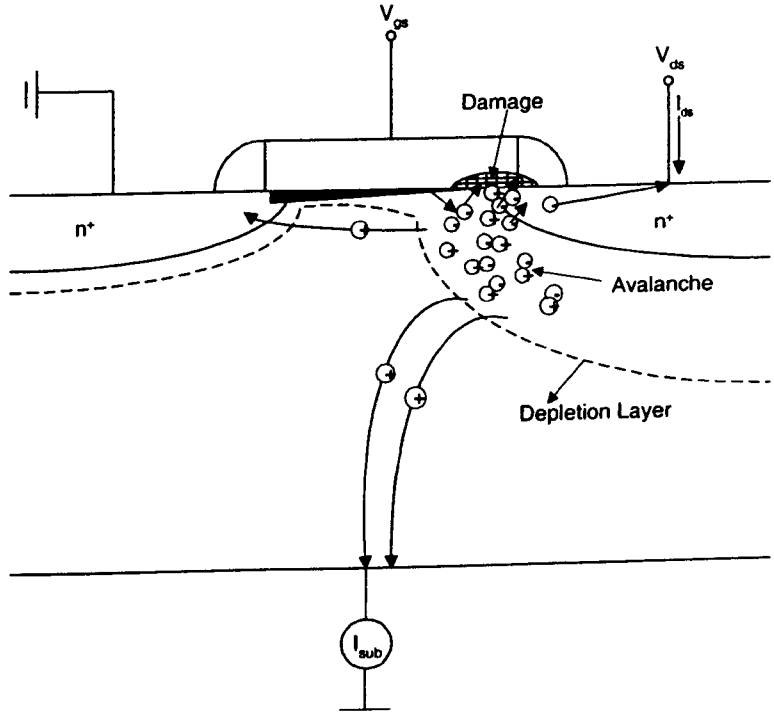


Fig. 3.3 Schematically shows hot carrier generation, injection and damage in the gate oxide.

Since the drain current is a measure of number electron entering saturation region, the number electron hole pairs generated as carriers travel a distance dx is given by product $I_{ds}\alpha dx$. The total substrate current is then given by integral [4]

$$I_{sub} = \int I_{ds}\alpha dx \tag{3.11}$$

Using (3.10) and (3.11) $I_{sub}$ can be expressed as [4]

$$I_{sub} = \frac{\alpha_i}{\beta_i} l E_m I_{ds} e^{-\beta_i / E_m} \tag{3.12}$$

where $E_m$ is the peak electric field given by (3.7) and parameter l is given by (3.5). Using values of parameters $\alpha_i$ and $\beta_i$, (3.12) can expressed as

$$I_{sub} = 1.2(V_{ds} - V_{dsat}) I_{ds} e^{-1.7 \times 10^6 / E_m} \tag{3.13}$$

Alternatively using lucky electron concept [4] the substrate current can also be derived. Assume that $\phi_i$ is the energy requited for impact ionisation then $\phi_i / qE_m$ is the distance that a

carrier must travel in order to gain this energy. The probability that the electron travelling in the electric field $E_m$ will gain energy $\phi_i$ is given by $e^{-\phi i/q\lambda Em}$, where $\lambda$ is electron mean free path. Since $I_{ds}$ is rate of supply of electron which can cause impact ionisation. The rate of the hot electrons having energy greater than $\phi_i$ is the substrate current and can be expressed as [8], [22]

$$I_{sub} = C_0 I_{ds} e^{-\phi_i / q\lambda E_m} \tag{3.14}$$

where $C_0$ is a constant. Eq. (3.14) is equivalent to (3.13) with parameter $\beta_i$ set as $\phi_i/q\lambda$ [8], [22]. Fig. 3.4 shows experimentally measured substrate current characteristics as function of the gate voltage for different values of the drain biases.

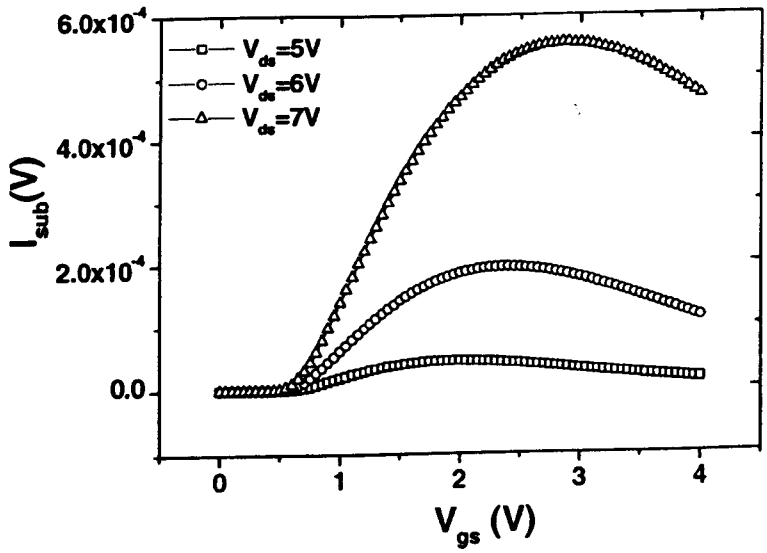


Fig.3.4 Substrate current as a function of the gate bias for different drain biases.

The bell shaped curve for $I_{sub}$ observed in Fig. 3.4 is due to the competing roles played by increasing $I_{ds}$ and decreasing lateral electric field as $V_{gs}$ is increased. It is noted from Fig. 3.4 that for given $V_{ds}$, as $V_{gs}$ increases $I_{ds}$ increases while $E_m$ reduces due to increase in $V_{dsat}$ leading two opposing factors. Initially at low gate biases substrate current first increases due to increase in $I_{ds}$. As $V_{gs}$ increased, $E_m$ decreases significantly leading to lower values of $\alpha$ and as result $I_{sub}$ decreases. The maximum in $I_{sub}$ is observed when product $I_{ds}\alpha$ is maximum.

### 3.4.2 Gate Current

The analytic gate current model based on lucky electron model was developed by Tam et. al [19]. For a hot carrier generated in the drain region to inject into the gate insulator must have an energy greater than Si-$SiO_2$ potential barrier $\Phi_b$. Assuming accelerating electric field to be $E_x$ the carrier must travel distance $\Phi_b/qE_x$ to gain this energy. In order to be injected into oxide the carrier must survive any scattering events from point of its generation in Si substrate until the interface. The probability that the carrier will travel distance d or more without suffering any energy loosing collision can be given as $e^{-d/\lambda}$, where $\lambda$ is carrier mean free path [23]. Therefore the probability that a carrier will acquire energy greater than $\Phi_b$ and inject into oxide is proportional to $e^{-\Phi b/qEx\lambda}$. Since $I_{ds}$ is rate of electron flow in the drain region, $I_{ds}e^{-\Phi b/qEx\lambda}$ is the fraction of total carriers in the drain region, which can inject into oxide. Following an analysis on similar lines as that for substrate current derivation (3.12), the gate current $I_g$, can be expressed as [19], [8]

$$I_g = C_1 F(E_{ox}) I_{ds} \left( \frac{q\lambda E_m}{\Phi_b} \right)^2 e^{-\Phi_b(E_{ox})/q\lambda E_m} \tag{3.15}$$

where $C_1$ is a constant, $F(E_{ox})$ is a function of the oxide electric field $E_{ox}$ and $\Phi_b(E_{ox})$ results from field dependence of barrier height due to Schottky effect also known as image force barrier lowering [17], [24]. The term $\Phi_b(E_{ox})$ has been modelled as [18]

$$\Phi_b(E_{ox}) = \Phi_{b0} - AE_{ox}^{1/2} - BE_{ox}^{2/3} \tag{3.16}$$

where A and B are coefficients whose values are $2.59\text{x}10^{-4}(\text{Vcm})^{1/2}$ and $4\text{x}10^{-4}\text{V}^{1/2}\text{cm}^{2/3}$ respectively [4]. Due to oxide field dependence of potential barrier for injection, the gate current in (3.15) is the gate also voltage dependent.

The direct measurement of the gate current is very difficult, since the typical gate current is limited to a few tenths of pico-Amps or below. This is especially true for the case of the hot hole gate current which is typically in femto-Amps range because of the higher barrier to hole injection at Si-$SiO_2$ interface (4.2eV as compared to 3.2eV for electron injection). In order to measure such low currents floating-gate technique has been widely used [25], [26]. In Fig. 3.5 a schematic representation of the gate voltage dependence of the gate current is shown. This dependence can be explained by considering Schottky effect and image band bending in

the substrate due to oxide field shown in Fig. 3.6 for $V_g<V_d$. At low gate voltages the field in oxide strongly favours hole injection.

The hole gate current is only measurable at very small $V_g$ ($V_g \sim V_t$) where the barrier height due to image force lowering is considerable. This is referred to hot hole injection region [9], [26]. As the gate voltage is increased the vertical field in the drain region decreases and enhancement of hole injection due to barrier lowering saturates.

However with increased $V_g$ the substrate current increases and the number of hot carriers generated also increase and electron injection starts to dominate. Therefore in the medium gate voltage range both electron and holes are simultaneously injected and the net measured gate current is zero around maximum substrate current ($V_g \sim V_d/3$-$V_d/2$) and is known as DAHC injection or $I_{submax}$ condition. On further increasing the gate voltage the oxide field favouring hole injection is reduced and the gate current starts to be dominated by electron injection. In this region a net electron gate current is observed which peaks around $V_g=V_d$ and is commonly referred to as electron injection condition [10], [21], [26]. When the gate voltage is increased beyond the drain voltage the measured gate current reduces due to reduction in generation of channel hot electrons. This happens due to the reduced lateral electric field at high vertical field as result of large gate bias.

## 3.5 Power Law Degradation and Life Time Prediction

The effect of the defects created by hot carriers in the oxide layer is felt on the electrical characteristics when they become charged. The most commonly measured device parameters, which are monitored for hot carrier degradation, are $g_m$, $V_t$ and $I_{ds}$. The degradation monitored in these parameters is used to device lifetime measurements.

### 3.5.1 Degradation of the Device Performance

The generated oxide charge leads to degradation of device characteristics both $I_{ds}$-$V_{ds}$, $I_{ds}$-$V_{gs}$ or transconductance, $g_m$. In Figs. 3.7(a) and 3.7(b) typical degradation of linear $I_{ds}$-$V_{gs}$ characteristics and transconductance are shown for a n-MOSFET 5V technology device before and after stress under $I_{submax}$ condition $V_d$=7V stressed for 1000s. It is seen that after stress both drain current and $g_m$ reduce.

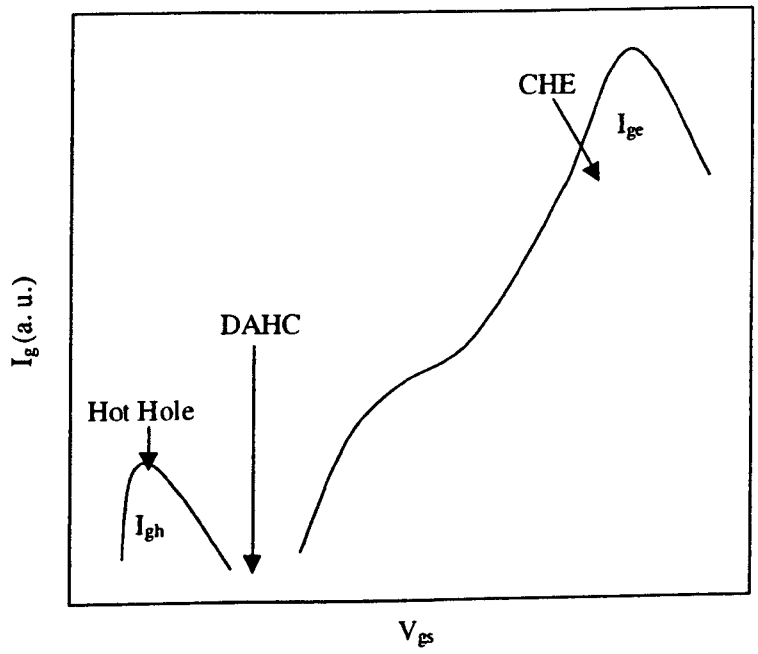


Fig. 3.5 Schematic representation of the gate current as function of the gate voltage for fixed $V_{ds}$.

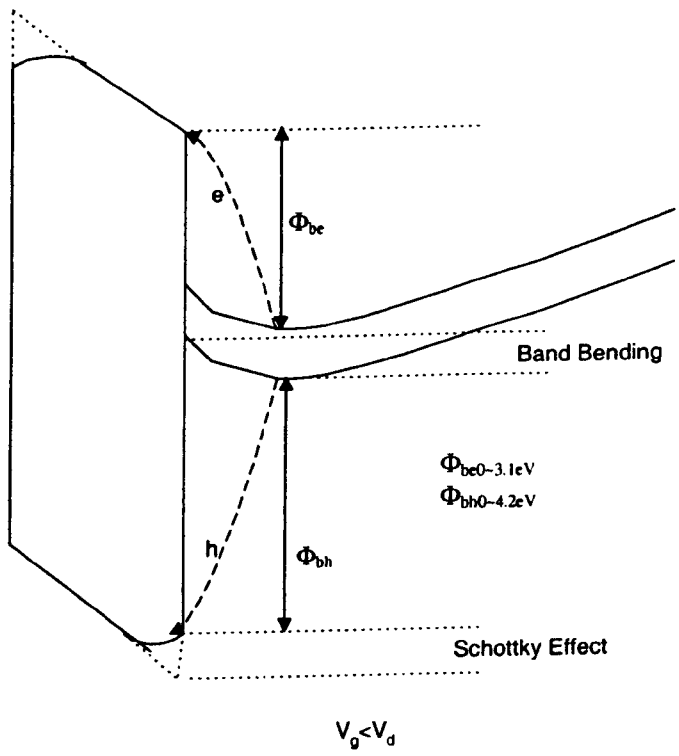


Fig. 3.6 Energy band diagram of n-MOSFET biased under $V_g<V_d$ condition showing barrier height lowering due to Schottky effect and band bending in Si substrate.

There are two basic mechanisms by which the device characteristics degrade. First the Coulombic scattering of the carriers in the inversion layer by oxide charge reduce the carrier mobility. Secondly the presence of net oxide charge shifts in device threshold voltage. The changes in both these parameters result in change in device currents according to (2.21) and (2.26). For the case for n-MOFESTs the damage in the form of acceptor type interface states, trapped positive and negative charge causes the shift in threshold voltage, mobility and subthreshold slope [8], [10], [21], [27]-[29].

For the case of lightly doped drain (LDD) technologies (to be discussed later) there is an additional degradation mechanism associated with series resistance increase due to damage in spacer region which has additional consequences for the degradation behaviour to be discussed in later [14], [30], [31].

### 3.5.2 Time Dependence of Degradation-Power Law Behaviour

The studies of time dependence of degradation of device parameters like transconductance ($g_m$), threshold voltage ($V_t$), the drain current ($I_{ds}$) show power law dependence [8]-[10], [32]. Fig. 3.8 shows an example of the time dependence of percentage transconductance $g_m$ degradation for 5V technology device stressed under $I_{submax}$ stress condition $V_d$=7V. It can be seen that the time dependence of degradation of device parameters follows power law behaviour

$$\Delta D = At^n \tag{3.17}$$

where $\Delta D$ is change device parameter e. g. $I_{ds}$, $g_m$, and $V_t$ etc., and A, n are constants. The parameter A depends on stress condition, process conditions and oxide quality [4]. The value of exponent n depends on stress condition and is 0.5-0.7 under $I_{submax}$ stress condition when degradation is dominated by interface state ($N_{it}$) generation [8]. Under $V_g \sim V_t$ and $V_g = V_d$ stress conditions the degradation has been reported be dominated by hole and electron trapping mechanisms respectively, the value of exponent n is found to lie between 0.2-0.3 [10], [21].

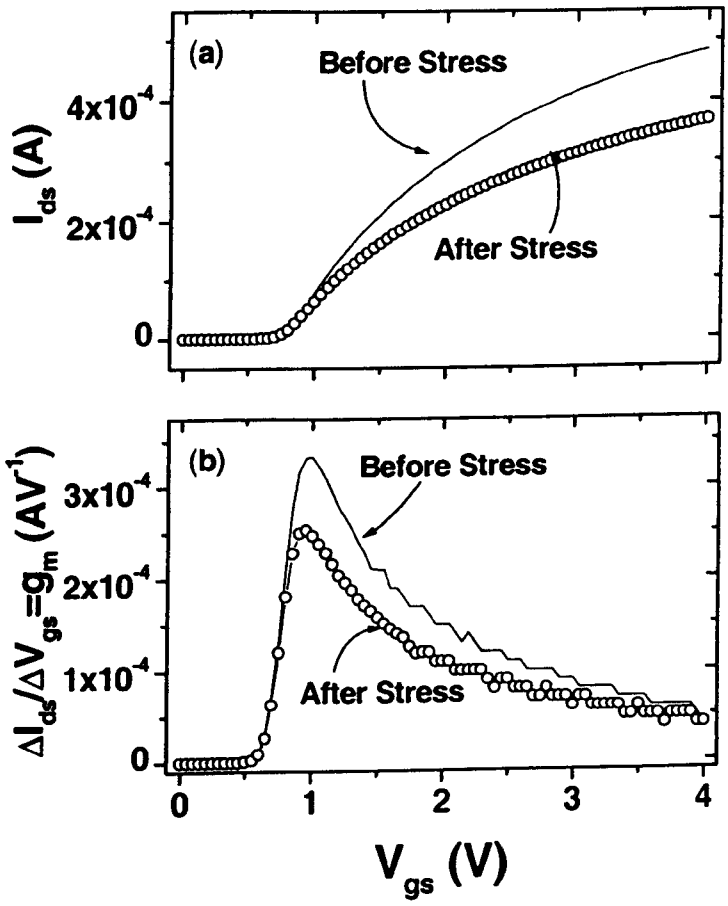


Fig. 3.7 Typical degradation behaviour of (a) linear $I_{ds}$-$V_{gs}$ characteristic and (b) corresponding transconductance degradation for 5V technology device stressed under $I_{submax}$ stress, $V_d$=7V, the stress time is 1000s.

However under all the stress condition it has been reported that interface generation follows power law with value of exponent n~0.5 [8], [10], [33]. This power law dependence of interface generation has been explained on the basis of hydrogen related species diffusion model [8].

### 3.5.3 Life Time Prediction

The lifetime in general is defined as the probability an item will perform a required function under stated conditions for a stated period of time. Translated to the context of MOS reliability, the lifetime is defined as time in which a device parameter will degrade by predefined amount generally 5-10%. The exact amount of degradation for lifetime prediction usually depends on the particular circuit design in which tolerance for parameter degradations is built-in. Since it is required to know lifetime before the device goes into circuit, so

accelerated ageing of the device is performed i.e., apply much higher voltages (stress) to get lifetime under stress and then project it to normal operating conditions. The most commonly used lifetime extraction technique was first reported by Takeda and Sezuki [32], which was refined later by Hu et. al. [8] and Bellen et. al. [11] based on a physical interpretation of the degradation mechanisms involved.

In this model degradation in the chosen device parameter is associated with generation of interface states ($\Delta N_{it}$) according to power law degradation behaviour [8]

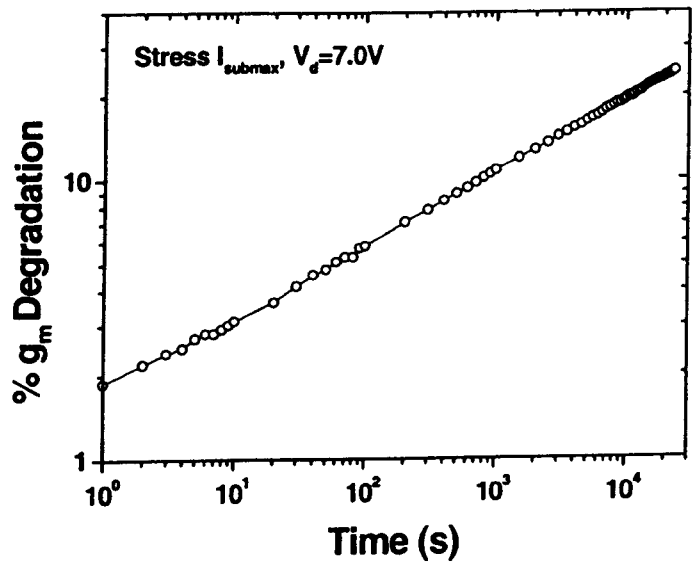


Fig. 3.8 Power law degradation behaviour.

$$\Delta N_{it} = C_1\left(t\frac{I_d}{W}\exp\left(\frac{-\phi_{it,e}}{q\lambda E_m}\right)\right)^n \tag{3.18}$$

where $\phi_{it,e}$ is the energy threshold for hot electron induced interface state generation and other parameters have same meaning as in (3.14). Eq. 3.18 also explains the power law dependence of parameter degradation as observed in Fig. 3.8 [8], [28]. By eliminating term $\lambda E_m$ in (3.18) using (3.13) and (3.12), (3.18) can be written as

$$\Delta N_{it} = \left[ \frac{I_d}{H_e W} \left( \frac{I_{sub}}{I_g} \right)^{\frac{\phi_{it,e}}{\phi_i}} t \right]^n \tag{3.19}$$

Where $H_e=C_0/C_1$. Defining $\tau$ as stress time to reach predefined amount $\Delta$ of degradation (3.19) can be rearranged as

$$\frac{\tau . I_{ds}}{W} = H_e \left( \frac{I_{sub}}{I_{ds}} \right)^{m_e}, m_e = \frac{\phi_{it,e}}{\phi_i} \tag{3.20}$$

where time $\tau$ is in seconds. By plotting term $\tau I_{ds}$ as function of $I_{sub}/I_{ds}$ on log-log scale yields straight line with slope roughly equal to m, while the intercept gives parameter $H_e$. A typical lifetime plot obtained using different combinations of the gate and the drain voltages using this procedure is shown in Fig. 3.9 [3]. It is noted in Fig. 3.9 that for values of $I_{sub}/I_{ds} < 8x10^{-2}$ the of slope m is –2.9. Assuming $\phi_i$~1.3eV the value of energy threshold $\phi_{it,e}$ for interface generation can be found to be equal to 3.7eV. This model supports well hot electron induced hydrogen release model for interface state generation [8] where energy threshold for $N_{it}$ generation can be interpreted in terms of energy required to overcome Si-$SiO_2$ barrier height (~3.2eV) plus energy required to break Si-H bond (0.3eV) [34]. Therefore this region of lifetime plot can be identified with interface trap generation dominated by electron injection.

Further, it is also noted in Fig. (3.9) that for higher values of $I_{sub}/I_{ds} > 8x10^{-2}$ the value of slope m is –5.5 and hot electron induced degradation model does not corresponds to right threshold for interface generation process in this region. It has been shown in [11] that the values of $I_{sub}/I_{ds} > 8x10^{-2}$ are in stress region where the lateral electric field is high. This corresponds to the low gate voltage ($V_g$~Vt) stress. Therefore degradation under this condition is dominated by interface state generation process by hot hole injection [33], [26]. For the generation of interface states by injected holes (3.20) has been modified to [10], [11]

$$\frac{\tau . I_{ds}}{W} = H_h \left( \frac{I_{sub}}{I_{ds}} \right)^{-m_h}, m_h = 1 + \frac{\phi_{it,h} \lambda_e}{\phi_i \lambda_h} \tag{3.21}$$

where $H_h$ is a technology dependent parameter, $\phi_{it,h}$ can be interpreted as energy threshold for interface generation by hot holes, $\lambda_e$ (~7.3nm) and $\lambda_h$ (~5.3nm) electron hole mean free paths respectively.

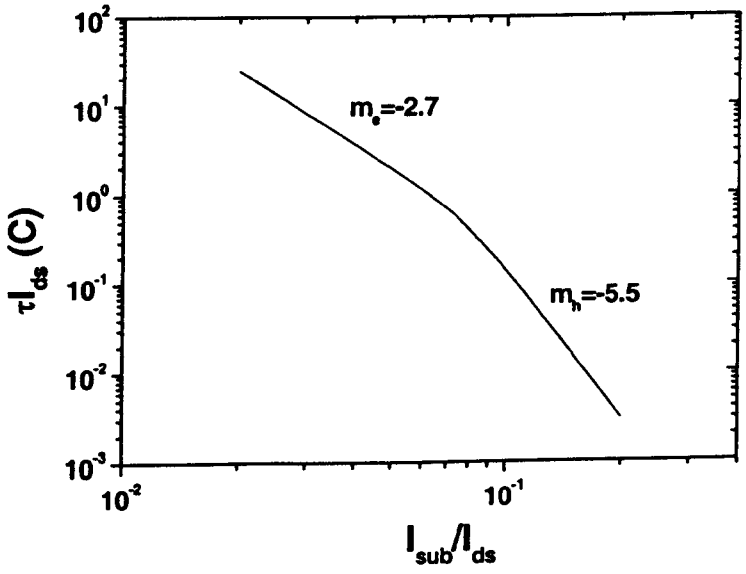


Fig. 3.9 Lifetime correlation plot with lifetime $\tau$ obtained from increase in $N_{it}$. At low $I_{sub}/I_{ds}$ a slope of –2.7 can be attributed to $N_{it}$ generation by electron injection, while at high $I_{sub}/I_{ds}$ the slope of –5.5 is due to $N_{it}$ generation by hole injection.

Using the value of the ratio $\lambda_h/\lambda_e$=0.724 [35], [3] the measured slope of –5.5 corresponds to $\phi_{it,h}$=4.2eV. This value agrees well with Si-$SiO_2$ barrier height for hole injection confirming hot hole induced interface state generation in this region.

Since $I_{ds}$ is proportional to W, (3.20) for the case of hot electron limited lifetime projection for wide range of technologies has been approximated by [4]

$$\tau = B\left[\frac{Isub}{W}\right]^{-3} \approx 3\left[\frac{I_{sub}}{I_{ds}}\right]^{-3} \qquad (3.22)$$

where parameter B is in general technology dependent.

Using above approach a general procedure for lifetime extraction for a particular technology under consideration can be summarised as:

1. Measure $I_{sub}/I_{ds}$ at operational voltage.

2. Using this value determine device lifetime from a correlation plot like shown in Fig. 3.9.

Conversely to find maximum allowable operating voltage for predefined amount of lifetime (say, $\tau$=10years):

1. Extrapolate lifetime plot to $\tau$=10years.

2. Determine $I_{sub}/I_{ds}$ at that time point.

3. Determine maximum supply voltage $V_{dd}$ from measured $I_{ds}$-$V_{ds}$ and $I_{sub}$-$V_{ds}$ characteristics.

## 3.6 Lightly Doped Drain (LDD) Devices

### 3.6.1 Need for Lightly Doped Drains

With channel length scaling there has been increase in the electric field in the device. This can be understood from (3.7), since scaling implies reduction in l through $t_{ox}$, $x_j$ and from (3.7) reduction in $V_{dsat}$ through L and $V_t$. If $V_{ds}$ in (3.7) is not scaled as much as required by constant field scaling laws, which usually has been the case [36], the peak electric field $E_m$ will increases. The increase in $E_m$ with scaling leads to serious hot carrier degradation for the device with effective channel length approaching 1μm to an extent that popular 10-year hot carrier lifetime criteria can no longer be met [13].

As an example taking a 1μm 5V technology (considered as conventional $n^+$ drain technology) studied in this work with $t_{ox}$=120Å, $x_j$=0.28μm, $V_{dd}$=5V, $V_t$=0.5V operating at $V_g$~$V_d$/2. Calculating $V_{dsat}$=1.33V from (3.6), $I_{sub}/I_{ds}$=0.013 from (3.13) gives lifetime of $\tau$~16days according to (3.22)! This is not clearly acceptable and highlights need for improved device structures if hot carrier reliability criteria is to be met. One way to alleviate this problem is to increase product $t_{ox}^{1/3}x_j^{1/2}$ but this in itself is against scaling principle and aggravates short channel effect like increased subthreshold slope, reduced punch through voltage in addition to reduced drive current and transconductance (via $C_{ox}$).

### 3.6.2 LDD Technologies for Lifetime Improvement

In order to overcome limitation posed by hot carrier degradation and enable scaling of devices in submicron regime Lightly Doped Drain (LDD), or graded drain doping MOSFET in general, have been proposed [12], [7], [37], [38]. The basic idea in these technologies is to

introduce a lightly doped $n^-$ buffer layer between the channel and $n^+$ drain as illustrated in Fig. 3.10 to reduce the peak electric field and consequently hot carrier generation. This buffer zone can be implemented with oxide spacer technology [39] or As-P double diffused junction [13].

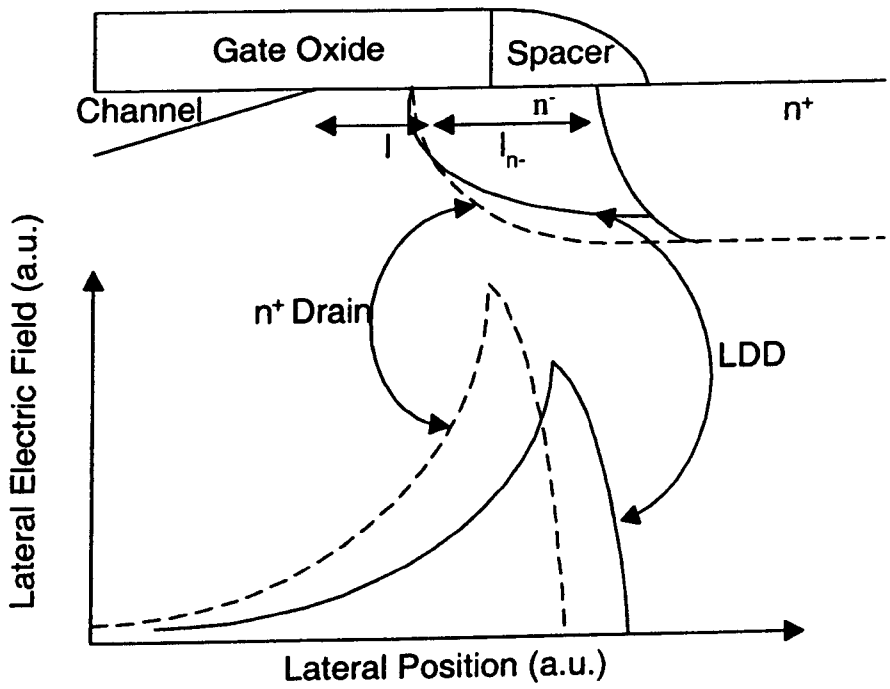


Fig. 3.10 Schematic illustration of LDD structure compared to conventional device and the resulting electric field profiles (not to the scale).

As seen in Fig. 3.10 for device operating in saturation (or in off state) the buffer layer supports the part of applied voltage drain voltage. This results in reduced electric field in saturation region shown in Fig. 3.10 by spreading it over larger distance as compared to conventional $n^+$ device.

An approximate expression for the peak electric field for LDD device can be obtained as follows [8]: Assuming that the electric field is constant over the length $l_{n-}$ of the buffer zone the additional voltage drop supported by this layer will be $E_m l_{n-}$, letting this voltage drop in (3.7), $E_m$ becomes

$$E_m = \frac{V_d - V_{dsat} - E_m l_{n-}}{l} \tag{3.23}$$

or

$$E_m = \frac{V_d - V_{dsat}}{l + l_{n-}} \tag{3.24}$$

Thus potential difference $V_{ds}$-$V_{dsat}$ is dropped across effective length of saturation region, l, plus length $l_{n-}$ of $n^-$ buffer region thereby reducing the peak electric field. In (3.23) it assumed that the electric field is constant over LDD length which is not true in general. Accurate analytic expression for the electric field for more realistic cases like Gaussian [40] and log-linear drain doping profiles has been obtained [41]. However the underlying concept in (3.24) holds true in general and (3.24) serves as an excellent guideline for quick evaluation of hot carrier performance of a LDD technology.

The reduced electric field in a LDD device has significant impact on hot carrier lifetime of a LDD device. To demonstrate considering 1μm technology case used above for $n^+$ drain device with a typical length of $n^-$ layer equal to 0.1μm. Using (3.13) $I_{sub}/I_{ds}$=0.00115 and (3.22) τ=61.94 years! This value is in stark contrast to mere 12 days obtained for a conventional technology with similar dimensions. Therefore use of the LDD technology offer real advantages in hot carrier reliability improvement. In addition the LDD technology also offers reduced short channel effects due to shallower $n^-$ layer junction as compared to conventional $n^+$ device [37].

### 3.6.3 Disadvantages of LDD Devices

Despite the distinct advantages an LDD technology offers over conventional technologies it also has its own disadvantages. In a conventional LDD device the $n^-$ drain offset is normally realised by spacer isolation process and $n^-$ region lies directly underneath spacer oxide (Fig. 3.10). The disadvantage of this kind of device structure is twofold.

Firstly, LDD devices have lower circuit performance compared to their conventional counterparts. This is because $n^-$ region has low drain doping and is not controllable by poly-Si gate, which results in increased series resistance. This leads to reduced current drive capability and lower transconductance $g_m$ compared to conventional devices. Typically 10-20% lower current and $g_m$ are obtained in LDD devices as compared to conventional devices [42]. In addition lower circuit performance also results from increased gate-drain/source parasitic capacitances [42].

Secondly, and more important from hot carrier point of view, although LDD device can be quite effective in reducing peak the electric field and substrate current an additional hot carrier degradation mode associated with series resistance increase exists in these devices [14], [43], [44]. Since concentration of the $n^-$ layer is lower compared to conventional devices any charge injection in spacer oxide causes depletion of underlying $n^-$ layer. As $n^-$ region is not under direct gate control its resistivity can increases quickly. The charge generated in spacer region depletes underlying $n^-$ drift layer forcing current away from the surface. As a result there is increase in the drain series resistance $\Delta R_{n-}$, which can be to a first order approximated as [14]

$$\Delta R_{n-} = \frac{\Delta L}{qW\mu_n(Q_n - \Delta N_{it})} \tag{3.25}$$

where $\Delta L$ is length of the damaged LDD region, $\mu_n$ is the electron mobility in LDD region, $Q_n$ is the LDD sheet charge density and $\Delta N_{it}$ is the increase in spacer charge density due to hot carriers stress and all other symbols have their usual meanings.

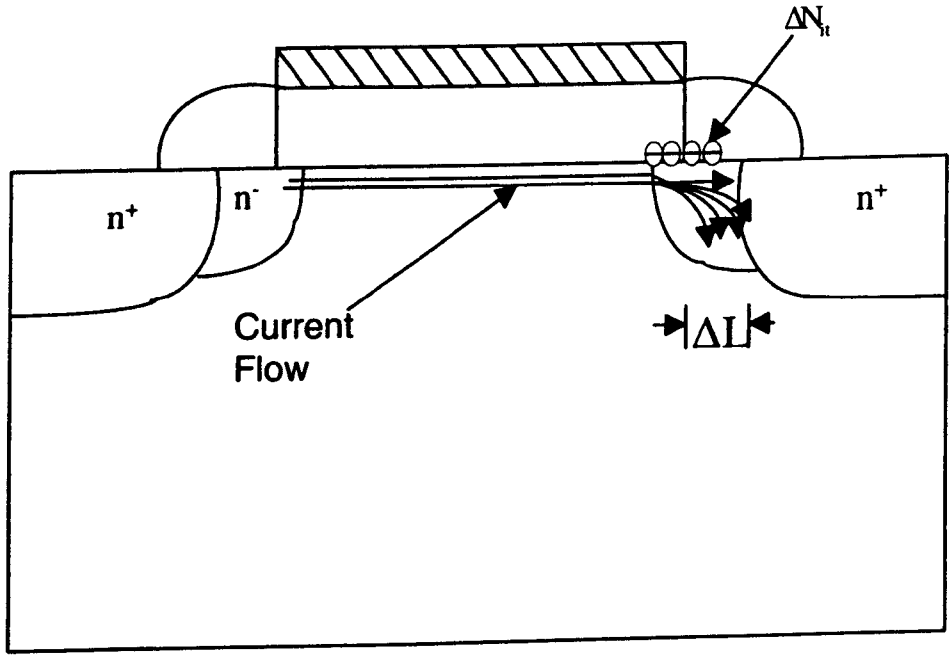


Fig. 3.11 Shows series resistance degradation associated with LDD device.

In addition since spacer oxide is formed by deposition process [39] it has inferior quality compared to thermally grown oxide. This can lead to a greater electron trapping or interface

state generation for modest amount of hot carrier injection [14], [43]. This causes additional susceptibility of these devices to hot carrier damage.

### 3.6.5 Improved Lightly Doped Drain Structures

As pointed in the previous section the main drawbacks associated with an LDD structure are reduced current drive due to increased series resistance and spacer induced degradation. These drawbacks can be overcome by optimising LDD doping profile. The aim is to increase the LDD doping to reduce the sensitivity of the LDD resistance to spacer charge. The LDD dose level in the range $5\text{-}6\text{x}10^{13}\text{cm}^{-2}$ has been used to achieve optimised LDD doping. In addition using higher LDD doping shifts the peak under or at the gate edge so that charge generation the spacer region is minimal [45]. The disadvantage of higher LDD doping is that the gate-drain/source capacitance will be higher compromising the circuit speed. Therefore in designing any LDD technology a trade-off between its performance and reliability is made and requires LDD doping profiles optimised to meet both of these requirements.

More recently many advanced drain-engineered structures have been proposed which overcome major drawbacks of conventional LDD technology. Central to all these new device concepts is to fully overlap the LDD drain by the gate. This keeps the peak electric field firmly under the gate or just at the gate edge, so that the spacer oxide is least exposed to hot carriers. Such structures are in general referred to fully overlapped LDD structures (FOLD). The examples of these devices include inverse-T gate LDD (ITLDD) [46], the gate drain overlapped device (GOLD) [47], fully overlapped nitride-etch defined (FOND) [48] and large angle tilted implant device (LATID) technologies [49]. The improved hot carrier lifetime in these structure is due to a combination of different factors which include: 1) location of the peak electric field under the gate, 2) direction of the current flow deeper into the saturation region to avoid the hot carrier generation near the interface, 3) pushing location of the peak electric field away from the interface and, 4) separating the majority of the current path in the drain region from location of the peak electric field.

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# CHAPTER 4

# MEASUREMENT SETUP, CHARACTERISATION AND DEVICE TECHNOLOGIES

## 4.1 Introduction

As described in Chapter 3, in the normal d. c. stress and measurement experiments the device is stressed at higher operating voltages for few thousand seconds or more to cause damage in the device at an accelerated rate. The resulting device degradation is monitored by carrying out a series of electrical measurements like I-V (linear and saturation), substrate current and charge pumping current. From these measurements degradation in the device parameters such as transconductance ($g_m$), threshold voltage ($V_t$), interface states ($N_{it}$) and series resistance ($R_{SD}$) can be monitored. This stress and characterisation sequence is usually referred to long term stress experiments and has been the focus of various studies for conventional and LDD technologies [1]-[6].

As outlined in Chapter 1, one of the aims of this study is to characterise the damage in the range of graded drain n-MOS technologies for very short stress time scale beginning from microseconds range, as well as under long term stress. In order to achieve stress time control for such a short time scale a special experimental setup is needed. This Chapter describes the special set-up implemented in this work to enable microsecond level d. c. stress and characterisation. Further this Chapter describes the different electrical measurements and characterisation methods used in this work to study the degradation under both short term and long term stress time scales. Finally the device details of different n-MOS technologies (LDD, MLDD, HDD) on which this work has been carried out on are presented.

## 4.2 Experimental Stress Sequence and Measurement

For studying hot carrier degradation under dc stress beginning from microsecond an experimental setup is needed in which both the gate and drain stress voltages are synchronised and stress time and terminal voltages are accurately controlled. Since it is intended to apply stress on very small stress time scales there is always possibility of transients or noise voltage being generated due to parasitic elements in the test circuit causing unwanted device degradation. In a typical experimental setup 50Ω coaxial cables are

commonly used to connect the device to supply voltages and these cables can have appreciable parasitic inductances. In the AC stress experiments which also involve applying stress for short periods by switching the device between on/off states at high gate frequencies with fixed DC drain voltage such transients have been reported [7]. It has been shown in these experiments that when the device is switched at high frequencies (~500kHz) by applying gate pulses, the parasitic inductance of source and drain cables can lead to generation of large transient or noise, $\Delta V$, in terminal voltages equal to

$$\Delta V = L\frac{dI}{dt} \tag{4.1}$$

where L is wiring inductance and I is the switched current. This noise voltage superimposed on actual stress voltage can cause enhanced device degradation [7]-[8]

To ensure that while applying stress voltages for small stress periods no setup related transients are generated (as in the case of AC stress experiments out lined above) causing spurious device degradation, an experimental setup with a special stress sequence is implemented in this work. A specialised HP16058A test fixture built for semiconductor component testing with dual-in-line package holder for packaged devices is used. The stress and measurement of devices are accomplished by using an HP4140B low current picoammeter (pA) unit and an HP8160A pulse generator unit (PGU). The entire stress and measurement cycle is implemented in LABVIEW graphics programming environment with GPIB bus. In the experiments the stress time is automatically controlled on a log scale.

In the test setup the voltage source VA of the pico-ammeter unit is used to apply the gate stress voltage and is also employed to trigger the PGU. The PGU trigger level is selected at gate stress voltage and is programmed to generate a single pulse of desired magnitude and duration. This single pulse, of duration which is the stress time for one stress cycle, is applied to the drain terminal of the device, while source and substrate terminal are held at external ground of the test fixture. The gate pulse is held on for approximately one second longer than the drain pulse. This stress sequence helps eliminate any noise voltage at source or drain terminals. Since the transient pulse voltage applied to drain is generated by the gate voltage, this insures that when the drain voltage is applied the device is in the on state. The long gate voltage rise time rate (~1V/s), short connecting cables and test fixture ground further help to reduce the transient noise voltages.

## 4.3 Test Circuit and Experimental Stress Voltage Waveforms

The basic schematic circuit for the experimental setup described in Sec. 4.2 is shown in Fig. 4.1. In the stress cycle the pA-VB arm of the circuit is switched off and PGU arm is switched on connecting the drain terminal to PGU. The VA source unit triggers the PGU, which generates a single pulse voltage of desired duration and magnitude. The source unit VA also applies the desired stress gate voltage $V_g$, while stress drain voltage $V_d$ is set by the triggered PGU. In the measure cycle the PGU is switched off and the drain terminal is connected to the pA-VB arm and the device $I_{ds}$-$V_{gs}$ characteristics in the linear region with low drain voltage $V_{ds}$=0.1V (set by VB) are measured.

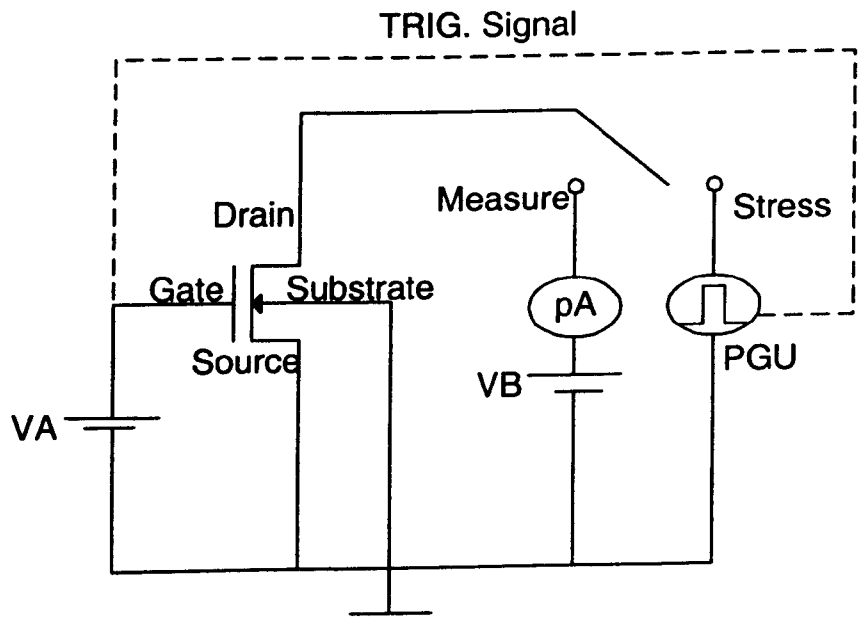



Fig. 4.1 Basic schematic of experimental circuit for the stress and measure cycles.

Figs. 4.2(a), 4.2(b) and 4.2(c) show the typical voltage waveforms measured at the gate and drain terminals under $I_{submax}$, $V_g$~$V_t$ and $V_g$=$V_d$ conditions respectively with the drain stress voltage $V_d$=7V. In this case a drain stress pulse for a period of 1μs is generated. Similar waveforms are obtained for other stress periods (not shown here). It is seen from Fig. 4.2 that with this setup and stress sequence a pure d. c. stress voltage of duration as low as 1 μs with negligible noise can be generated. The drain stress pulse is generated when the gate stress voltage for the corresponding stress condition is reached. This insures a good synchronisation of the gate and drain stress voltages resulting in accurately controllable stress drain voltage.

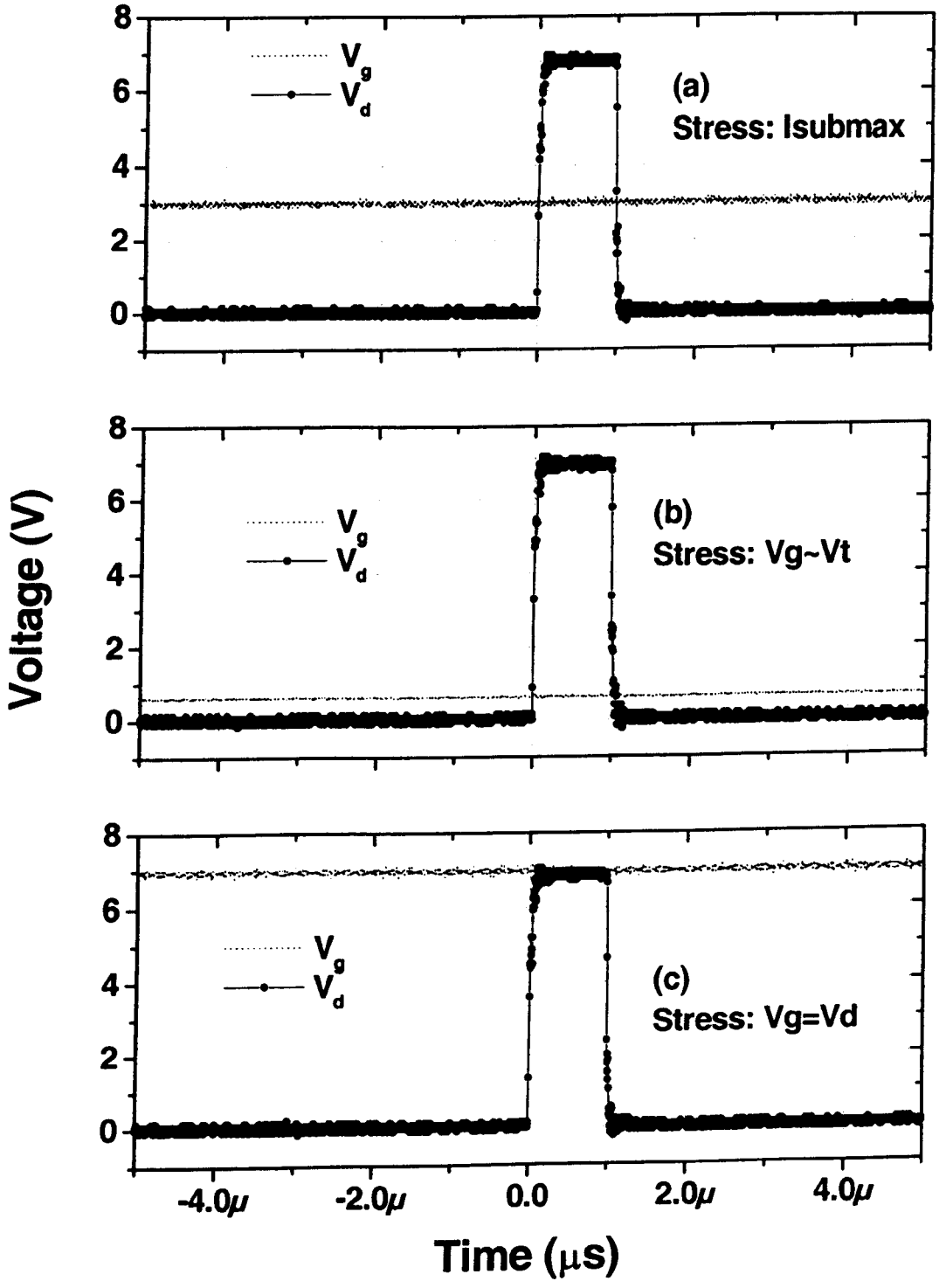



Fig. 4.2 Measured gate (thin dotted lines) and drain (thick solid line connecting circles) waveforms for drain stress bias $V_d$=7V of 1μs duration under (a) $I_{submax}$, (b) $V_g$~$V_t$ and (c) $V_g$=$V_d$ stress conditions.

## 4.4 Automated Measurement Setup

In order to achieve a good repeatability and efficiency of measurements an automated measurement setup is integrated with test setup as described in Secs. 4.2 and 4.3. This expanded setup enables stress and different measurements to be carried out on the device under test (DUT). It is achieved using a Keithley 7001 switching system with a 4x5 low leakage 7152 switching matrix. The use of a switching system enhances the functionality of the test setup, and allows to perform stress as well as more than one characterisations without having to manually change the test connections. In Fig. 4.3 a generalised block diagram of this setup is shown.

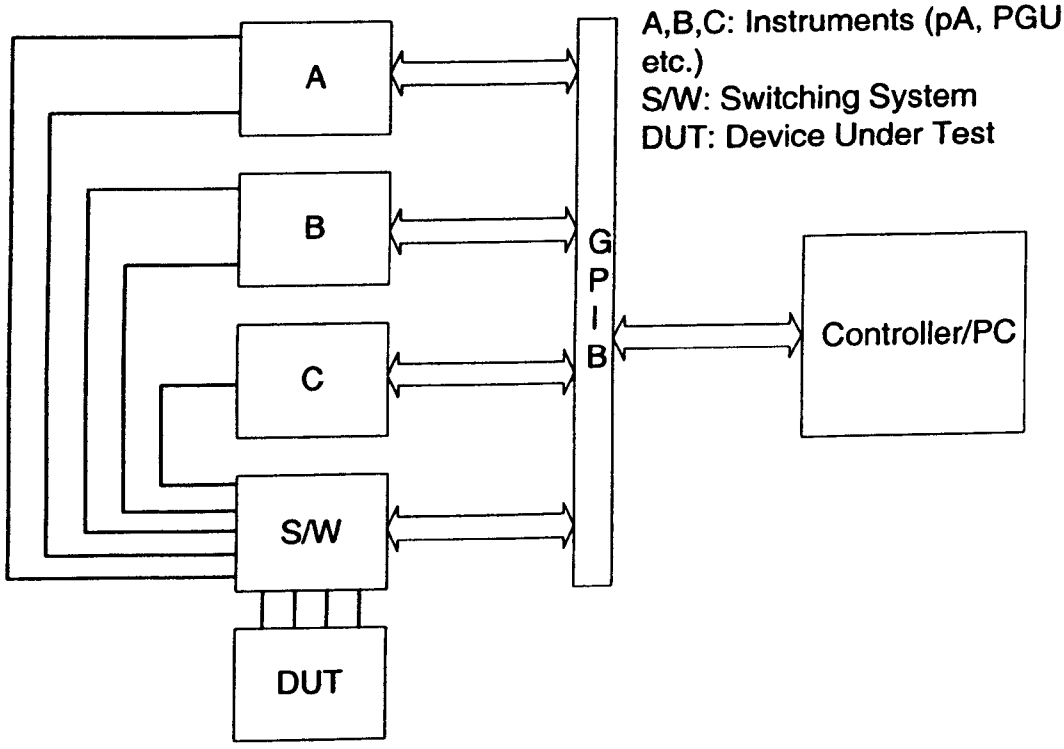
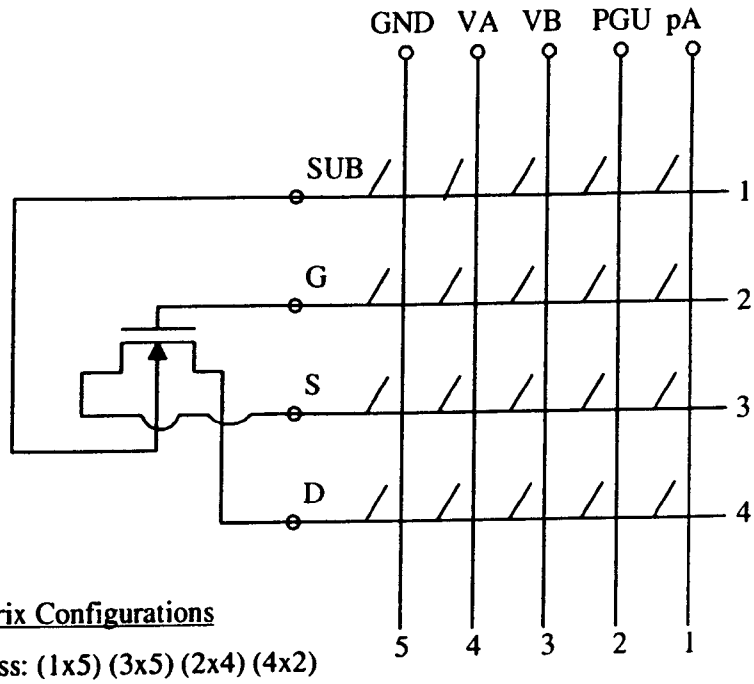



Fig. 4.3 Block diagram of the automated experimental setup.

In Fig. 4.3 the different electrical systems like the HP4140B pA unit, PGU, Keithley 7001 switching system are connected to a common PC controlled GPIB interface. The outputs from source units are connected to columns of the switching matrix while rows are connected to device terminals. The outputs from these instruments are switched to rows connected to source, drain, gate and substrate terminals. The switching configurations of the matrix will

depend in general on the type of measurement performed. Fig. 4.4 shows switching matrix configurations for stress, $I_{ds}$-$V_{gs}$ and charge pumping ($I_{cp}$) measurements using the 4140B and PGU units employed in this work.




Matrix Configurations

Stress: (1x5) (3x5) (2x4) (4x2)

$I_d$-$V_g$: (1x5) (3x1) (2x4) (4x3)

$I_{cp}$: (1x1) (5x3) (2x2) (5x4)

Fig. 4.4 Automated measurement set-up using switching matrix to carry out multiple type measurements used in this work.

In Fig. 4.4 the PGU and source units VA of the 4140B are used to stress the device, source units VA, VB and the pA unit of the 4140B are used for I-V measurement and the pA and PGU unit are used for charge pumping measurements. The automated program to perform stress and desired measurement has been implemented in LABVIEW graphics programming language. The program automatically controls the switching configurations and all the other aspects of the stress and measurements.

## 4.5 Characterisation Techniques

The injection of electron and/or holes causes damage to the gate oxide in the form of trapped charge and interface states. In the early studies of the degradation behaviour of conventional n-MOS technologies the degradation of transconductance, threshold voltage or interface

charge measurement using charge pumping measurement were used as monitors of degradation [1]-[3].

However with the introduction of LDD technologies, additional degradation mechanism related to the increases in drain series resistance has lead to introduction of methods to monitor this form of the degradation. These include monitoring linear drain current at high gate voltage when the channel resistance is lower compared to series source-drain resistance [5], [8], direct monitoring of series resistance increase using the L-Array method and methods based on device characteristics measured in forward and reverse mode of operation [6], [9]. In addition there have also been studies aimed at monitoring the damage in the LDD region using charge pumping measurements [8], [10]. This section reviews the characterisation method used to monitor the LDD damage using both linear region drain current degradation and charge pumping measurements.

### 4.5.1 Drain Current Characteristics

Both transfer characteristics (linear $I_{ds}$-$V_{gs}$ at $V_{ds}$~0.1) and forward characteristics have been used to characterise the hot carrier damage after the stress [11]. But measurement of linear characteristics is normally preferred over forward characteristics. This is due to two reasons:

1) The measurement of forward characteristics involves the device operation in the saturation region, which in itself can cause finite device degradation leading to erroneous measurement of degradation of the device parameters, especially when degradation caused by stress itself is small.

2) As the damage in the device is localised in the drain region, operating the device in saturation region reduces the effect of the oxide charge on drain current [12]. Since the carriers in the saturation (or pinchoff) region of the device are not confined to the surface, the affect of the damage in this region on carriers is greatly reduced. This results in lower measured damage than is actually present.

The measurement of linear characteristics eliminates both of these disadvantages, as no saturation is present in this case. From the change in linear $I_{ds}$-$V_{gs}$ characteristics, degradation in mobility and the series resistance can be extracted using L-array method [6]. A methodology for analysing the degradation behaviour using this technique is presented in Chapter 6.

### 4.5.2 Charge Pumping

Apart from monitoring the degradation in device parameters extracted from I-V characteristics as discussed above another method, which has proved very useful in monitoring the degradation, is the charge pumping technique [4]. This method yields direct information on the nature of the damage in the oxide. This section reviews the basic principle of charge pumping techniques, different variations of the charge pumping method and its application as a tool to study the hot carrier damage in MOSFETs. This technique has been utilised in later Chapters for the analysis of the degradation behaviour after stress.

#### 4.5.2.1 The Basic Principle

The basic setup for charge pumping method for the case of an n-channel device is shown in Fig. 4.4 [4]. The source and drain are connected together and held at a small reverse bias or grounded. The gate of the transistor is connected to the pulse generator unit and a series of pulses of frequency f, base voltage ($V_{base}$) and top voltage ($V_{top}$) are applied.

The "charge pumping effect" occurs because of the recombination of electrons and holes at the interface as surface potential is alternated between inversion and accumulation by applied gate pulses. When $V_{top}$ is higher than the threshold voltage $V_t$, the surface is inverted and interface states are filled with electrons. When the base gate voltage $V_{base}$ is lower that flatband voltage $V_{fb}$ the surface is accumulated and holes combine with electrons trapped at interface at a rate given by frequency f of the applied gate pulse. This results in the charge pumping effect. The sequence depicting the charge pumping effect for one gate voltage cycle and the corresponding band diagrams are shown in Fig. 4.5.

The recombination of electrons and holes during one complete cycle is collected at the substrate as charge pumping current called $I_{cp}$. The interface charge, which recombines in one cycle is proportional to interface state density and is given by [4]

$$Q_{ss} = A_g q \int D_{it}(E) dE \qquad (4.2)$$

where $A_g$ is the gate area, q is the electronic charge, $D_{it}$ is the interface state density (measured in $eV^{-1}cm^{-2}$) and E is the energy.

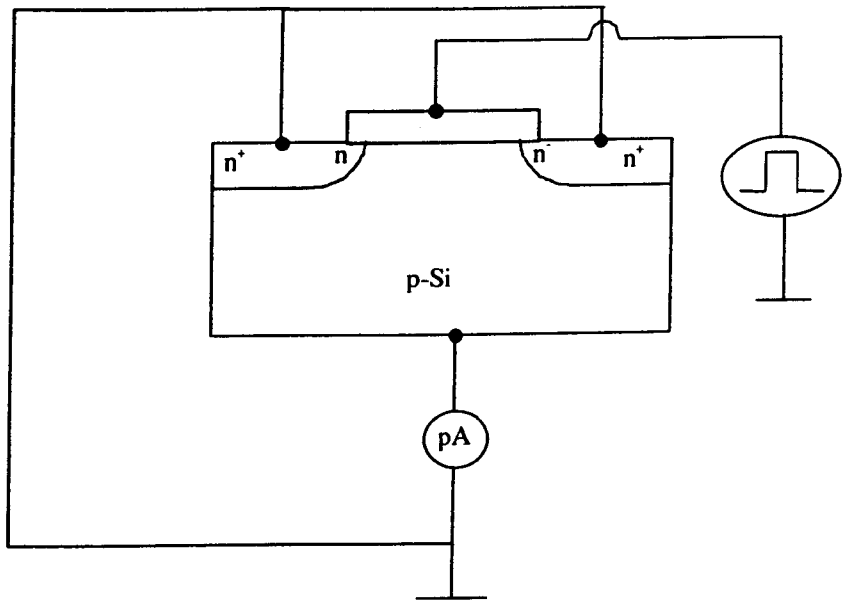



Fig. 4.4 Schematic diagram of charge pumping setup.

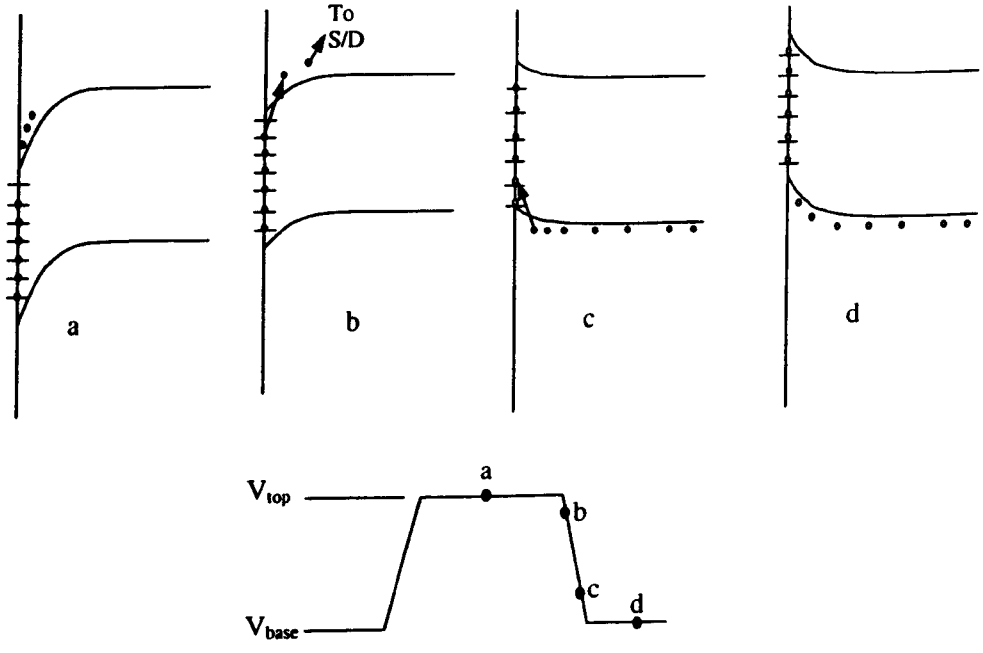



Fig. 4.5 Shows the energy band diagrams during the different stages when the gate pulse goes from high to low: (a) inversion and filling of the interface states by electrons (b) near the flatband condition, when the majority of the electrons remain trapped in the interface states (c) weak accumulation, holes start to recombine with the trapped electrons (d) all the trapped electrons are filled by the holes.

Assuming the mean interface state density of $<D_{it}>$ and energy range in the bandgap $\Delta E=q\Delta\psi_s$ over which interface charge recombination occurs, where $\Delta\psi_s$ is surface potential sweep between accumulation and inversion, the recombination charge $Q_{ss}$ and the charge pumping current $I_{cp}$ can be expressed as

$$Q_{ss} = A_g q^2 < D_{it} > \Delta\psi_s \tag{4.3}$$

$$I_{cp} = fA_g qN_{it} \tag{4.4}$$

where $N_{it}=q<D_{it}>\Delta\psi_s$ is the number of interface states per unit area. The energy interval in the bandgap $\Delta E$ which contributes to charge pumping current in general depends on electron and hole capture corrections $\sigma_e$ and $\sigma_h$ respectively, and time $t_e$, $t_h$ available for electrons and holes emission from interface states when the surface changes from inversion to accumulation and visa-versa [4]. The values $t_e$ and $t_h$ depend on the rise and fall time of the applied gate pulse. The general expression for $I_{cp}$ is given by [4]:

$$I_{cp} = fA_g 2q < D_{it} > kT \ln[v_{th} n_i (\sigma_e \sigma_h)^{1/2} (t_e t_h)^{1/2}] \tag{4.5}$$

### 4.5.2.2 Constant Amplitude Charge Pumping Method

In this method the values of $V_{top}$ and $V_{base}$ are varied to keep the gate pulse amplitude constant, while $V_{top}$ is swept from deep in accumulation to deep in inversion. The characteristic charge pumping curve for varying $V_{base}$ and the corresponding pulse levels in different regions is shown in Fig. 4.6. It is noted that for the case of n-channel devices as long as $V_{top}$ and $V_{base}$ are lower than channel threshold voltage, $V_t$, or $V_{top}$ and $V_{base}$ are higher than the channel flatband voltage $V_{fb}$, $I_{cp}$ is zero. Since for the former case no inversion takes place and for the later case there is no accumulation, so the net recombination at the interface is zero. The charge pumping current is maximum, $I_{cp,max}$, when $V_{top}$ is larger that $V_t$ and $V_{base}$ is lower that $V_{fb}$. In this case the entire interface along the channel is swept from accumulation to inversion when the gate voltage goes from $V_{base}$ to $V_{top}$ and converse, resulting in full charge recombination at the interface.

The transition regions in $I_{cp}$ values from low to high and high to low as seen in Fig. 4.6 are caused by $I_{cp}$ contribution from gate drain and source (LDD, or n+) overlap regions. Since, from channel to source/drain regions the threshold voltage ($V_t$) and flatband voltages are

decreasing from maximum value in channel to minimum value corresponding to $n^+$ source/drain regions, as illustrated in Fig. 4.7 for one junction.

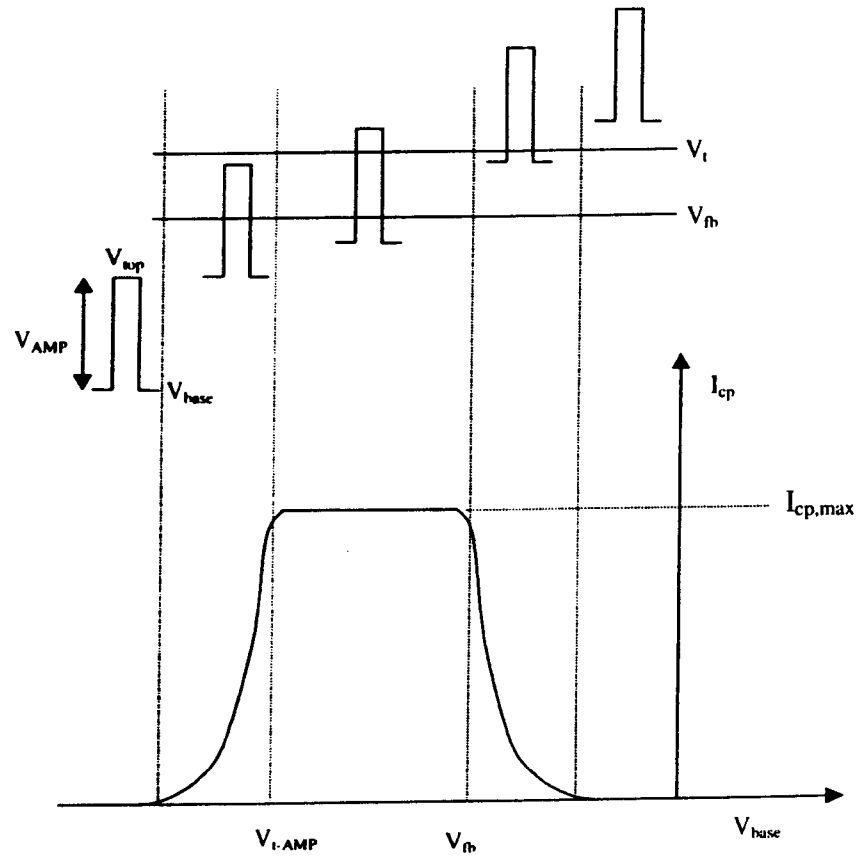



Fig. 4.6 Schematic representation of n-channel constant base charge pumping characteristics, $V_t$ and $V_{fb}$ are channel threshold and flatband voltages respectively.

Therefore, even when $V_{base}<V_t-V_{AMP}$, there is a region under the gate and source/drain overlaps where $V_{top}$ is greater than the local threshold voltage and $V_{base}$ is lower than the local flatband voltage, marked by length $\Delta L/2$ in Fig. 4.7. So, $I_{cp}$ current contribution leading to rising transition region seen in Fig. 4.6 is obtained. Similar reasoning applies to the falling transition edge in Fig. 4.6, here for $V_{base}>V_{fb}$ there are regions under the gate and source/drain overlaps where $V_{base}$ will be lower than the local flatband voltage leading to a falling edge in the transition region in Fig. 4.6. The slope of transition region in general depends on doping gradient of source and drain regions, the higher the LDD doping the sharper the rise and fall in the transition regions [4], [11]. The general expression for $I_{cp}$ for any pair of $V_{base}$ and $V_{top}$, assuming that $\Delta L$ is corresponding length of interface contributing to charge pumping current, can be written as [4], [10]

$$I_{cp} = qfW\Delta LN_{it} \tag{4.6}$$

where W is device width. The value of maximum charge pumping current $I_{cp,max}$ in Fig. 4.6 is approached when $\Delta L \rightarrow L_{eff}$ (effective channel length) and is given by

$$I_{cp,max} = qfWL_{eff}N_{it} \tag{4.7}$$

If the physical overlap region between the gate and source/drain is small compared to channel, $L_{eff}$ in (4.7) can be to first order replaced by the drawn gate length.

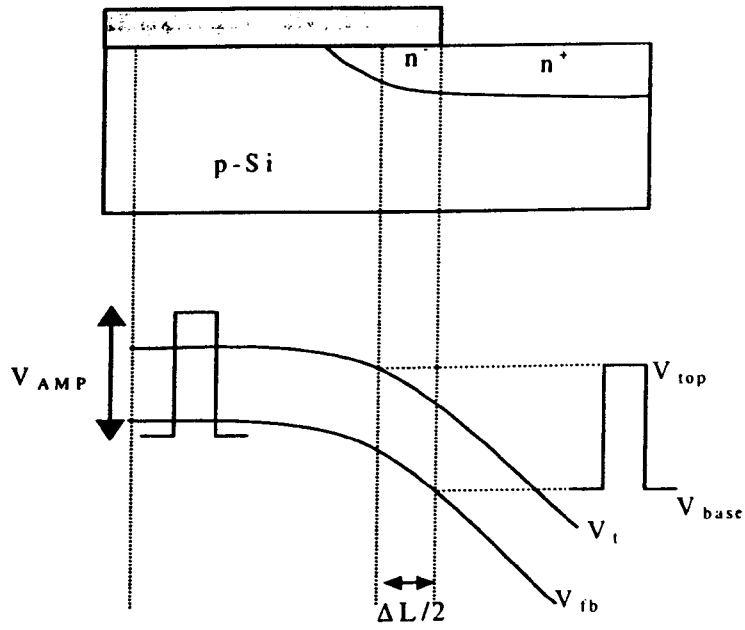



Fig. 4.7 shows charge pumping of source drain regions.

### 4.5.2.3 Constant Base Charge Pumping Method

In this method the base pulse gate voltage is fixed at a sufficiently low value while $V_{top}$ is varied from a low value to value greater than or equal to channel threshold voltage ($V_t$) [10]-[13]. The schematic characteristics for constant base charge pumping is shown in Fig. 4.8. For $V_{top}$ lower than $V_t$, the charge pumping region is confined to source drain overlap regions. The interface region contributing to the charge pumping current is determined by two points along the interface for which $V_{top}$ is greater than or equal to the local threshold voltage and $V_{base}$ is less that or equal to local flatband voltage, similar to the region marked by length $\Delta L/2$ in Fig. 4.7.

As $V_{top}$ is increased the region of interface contributing to $I_{cp}$ start to increase from deep in source/drain regions towards the channel region and the charge pumping current starts to increase. When $V_{top}$ becomes greater than or equal to channel threshold voltage $V_t$, $I_{cp}$ saturates and can be approximated by [10]

$$I_{cp,max} = qfW(L_{eff} + \Delta L_{ov})N_{it} \tag{4.8}$$

where $\Delta L_{ov}$ is the length of interface in the source/drain regions contributing to $I_{cp}$ and is slightly larger than the actual source drain overlap length due to charge pumping current contributed by spacer region [8]. But to a first order it can be approximated as the gate source/drain overlap length.

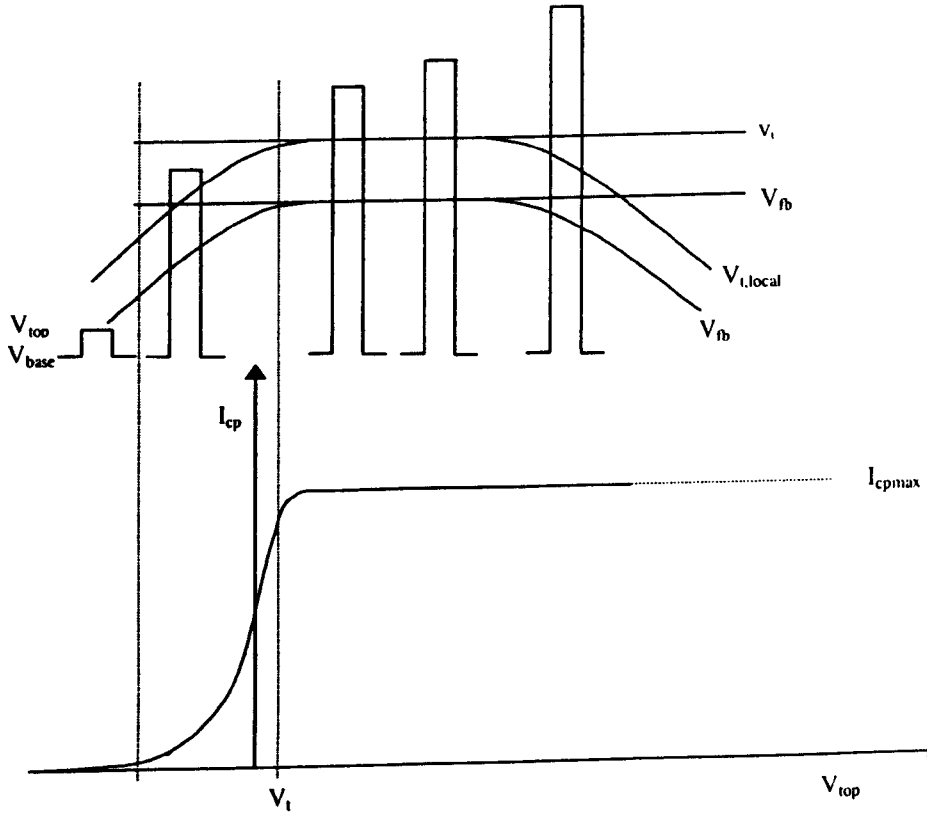



Fig. 4.8 Illustrates the schematics of constant base charge pumping characteristics.

### 4.5.2.4 Application of Charge Pumping Method to Hot Carrier Characterisation

Both constant amplitude and constant base charge pumping techniques can be used for characterising interface states and oxide charge created after stress. These methods have been used for lateral profiling of interface and fixed oxide charge [12]-[15]. In this section a

method to find trapped charge and increase in interface states after hot carrier stress is described.

The application of hot carrier stress to device leads to the creation of localised damage region near the gate/drain overlap, which leads to a change in $I_{cp}$ after stress. Increase in saturation charge pumping current can be directly used to find an average increase in the density of interface states, $\Delta N_{it}$, after stress using (4.6)

$$\Delta N_{it} = \frac{\Delta I_{cp,max}}{qfW\Delta L_d} \tag{4.9}$$

where $\Delta I_{cp,max}$ is increase in saturation charge pumping current and $\Delta L_d$ is the length of the interface region damaged by stress which can be approximated as width of peak electric field profile for a particular stress conditions.

The creation of fixed charge after stress leads to a shift in the charge pumping curve along x-axis in Fig. 4.8 [4], [12]. When positive charge is created the curve in Fig. 4.8 shifts to the left due to reduced local threshold voltage and when negative charge is created the curve in Fig. 4.8 shifts to the right due to an increased threshold voltage. In addition the creation of interface states in a stressed device also leads to a left shift in $I_{cp}$ curve in Fig. 4.8. The resulting change in charge pumping characteristics is shown in Fig. 4.9.

So any shift in $I_{cp}$ characteristics after stress is in general a result of damage caused both by interface states and trapped charge. In order to estimate the trapped charge a charge neutralisation procedure, where charge of opposite polarity to the trapped charge are injected by applying appropriate stress voltages, is performed [12]. After injection the $I_{cp}$ curve normally recovers as shown in Fig. 4.9 for the case of positive charge after stress, neutralised by negative injected charge.

From Fig. 4.9 the shift, $\Delta V$, in $I_{cp}$ curve after electron injection for a stressed device where positive charge has been created can be used to get find positive trapped charge, $Q_{ot}$, created after stress by following relation [12]

$$Q_{ot} = C_{ox}\Delta V / q \tag{4.10}$$

where $C_{ox}$ is oxide capacitance per unit area. Similar arguments apply to the case when the negative charge is created after stress.

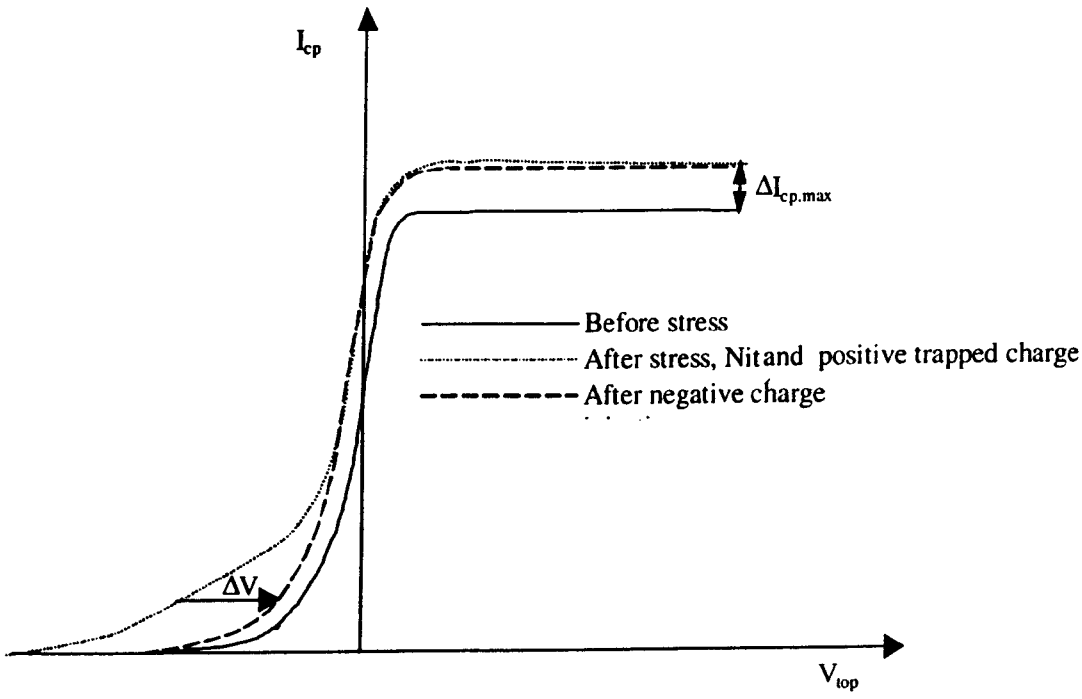



Fig. 4.9 Behaviour of the constant base charge pumping characteristics after positive charge and interface state creation and subsequent neutralisation using electron injection.

## 4.6 Details of the Device Technologies

The devices used in this study are n-MOSFETs, $n^+$ poly-Si gate belonging to different generation of technologies, optimised for 5V, 3V and 2V operation. The devices have a width of 15μm. Table 4.1 summarises the different structural parameters for a particular technology. In these technologies the conventional spacer isolation process is used in the $n^-$ and $n^+$ drain formation and is deposited from TEOS source.

The drain doping in the spacer region is low to moderate for 5V, 3V technologies. So these technologies have been referred to as lightly doped drains (LDD, 5V) and moderately doped drains (MLDD, 3V). For 2V technology the drain doping in the spacer region is very high reaching $1x10^{18}$ $cm^{-3}$ and has been referred to highly doped drain (HDD). It should be mentioned that for all the devices the drain doping in the transition $n^-$ region from channel to $n^+$ drain is highly non-uniform and the values given in Table 4.1 are approximate figures in the spacer region, where high electric field under stress is found from the simulations.

Table 4.1

| **Technology** | **Mask Length, L (μm)** | **Effective Channel Length, $L_{eff}$ (μm)** | **Oxide Thickness, $t_{ox}$ (Å)** | $N_{sub}$ ($cm^{-3}$) | $N_{LDD}$ ($cm^{-3}$) | $x_j$ (μm) |
|---|---|---|---|---|---|---|
| 5V (LDD) | 0.48-0.55 | 0.3-0.35 | 110-120 | $1x10^{17}$ | $1-2x10^{17}$ | 0.30 |
| 3V (LDD) | 0.36 | 0.3 | 58-65 | $3-4x10^{17}$ | $4-5x10^{17}$ | 0.22 |
| 2V (HDD) | 0.32 | 0.25 | 55-58 | $5x10^{17}$ | $8-10x10^{17}$ | 0.18 |

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# CHAPTER 5

# EARLY STAGE HOT CARRIER DEGRADATION

## 5.1 Introduction

It is well known that high electric fields occurring at the drain junction of sub-micron MOSFETs cause hot carrier degradation of devices. The ageing is caused either due to generation of interface states at the silicon-silicon dioxide interface [1]-[3], trapping of hot carriers in the oxide [4], [5] or a combination of both. The gradual deterioration in the transistor characteristics affects device lifetime and circuit reliability. Hence the prediction, understanding and control of this phenomenon are important issues in very large scale integration (VLSI) technology.

As summarised in Chapter 3 the long-term degradation behaviour of conventional devices has been well studied and lifetime prediction models well established [1], [6], [7]. However the lightly doped drain (LDD) technologies show degradation behaviour that is markedly different from that of conventional $n^+$ drain devices [8]-[12]. In that it has been reported that these technologies show a two stage saturating/self-limiting behaviour observed after long stress periods [8], [12], [13]. Since spacer region plays a significant role in determining device degradation behaviour, studying the degradation of experimentally measured parameters will help to qualitatively estimate its role in the device degradation. In particular since the spacer region is very sensitive to the minute amount of hot carriers injection, stressing the device for very short stress time scales will quantify the sensitivity of a particular technology to this type of damage. Further from the point of view of technology qualification and reliability prediction, it is equally important to study and understand the effect of device scaling on device degradation behaviour.

As pointed out in Chapter 1, one of the objectives of this work is to study the device degradation behaviour for short stress time and its long-term evolution. This will allow an understanding of initiation of hot carrier damage in these technologies and subsequent behaviour of the damage under long-term stress. This Chapter presents the experimental results of the degradation behaviour of 5V, 3V and 2V technologies whose details are given

in Table 4.1. The devices are stressed under $V_g \sim V_t$, $I_{subamax}$ and $V_g=V_d$ stress conditions with stress time beginning from microseconds. The stress and characterisation is performed using experimental stress setup described in Chapter 4. The degradation after stress is analysed by studying maximum transconductance $g_m=dI_{ds}/dV_{gs}$ obtained from measured linear $I_{ds}$-$V_{gs}$ characteristics at $V_{ds}=0.1V$ and linearly extrapolated threshold voltage $V_t$.

## 5.2 Degradation Behaviour of 5V Technologies

### 5.2.1 Transconductance ($g_m$) Degradation

Figs. 5.1, 5.2 and 5.3 show maximum transconductance $g_m$ degradation behaviour for 5V devices with effective channel lengths 0.5μm and 0.55μm under $I_{submax}$, $V_g \sim V_t$ and $V_g=V_d$ stress conditions. From Fig. 5.1, 5.2 and 5.3, a deviation from the normal power law degradation at stress time less that 100ms is apparent. The characteristic can be clearly divided into two regimes.

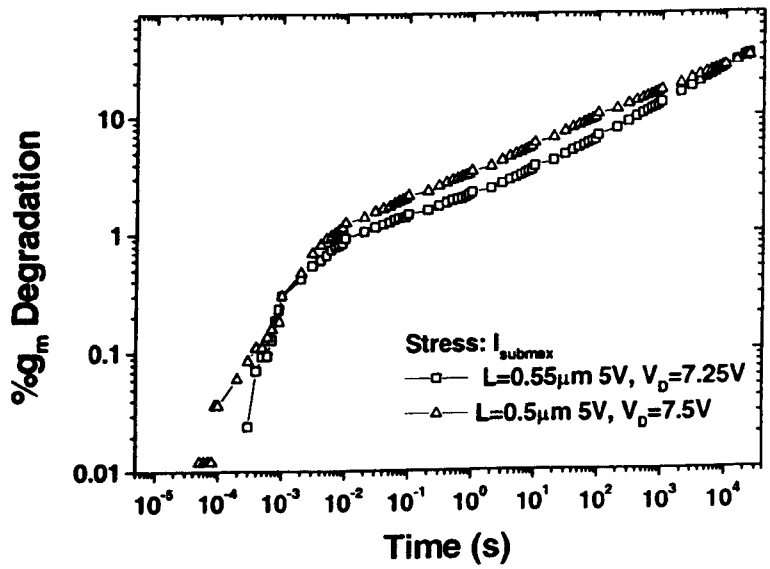


Fig. 5.1 Maximum transconductance ($g_m$) degradation behaviour for 0.55μm, 5V and 0.5μm, 5V technologies. The devices are stress under $I_{submax}$ conditions: ($V_d$=7.25V, $V_g$=2.9V, $V_d$=7.5V, $V_g$=3.1V).

It is noted that for all the stress conditions the initial rise in the degradation lasting up to 0.01-0.1 seconds is sharp, with slopes of 0.7-0.9 under $I_{submax}$, 0.5-0.6 under $V_g=V_t$ and 0.45-0.6 under $V_g=V_d$ conditions. In the second stage which corresponds to normally observed power law behaviour there is a reduction of slopes to 0.2-0.28 for $I_{submax}$ and $V_g=V_t$ conditions following power law degradation behaviour.

However it is noted from Fig. 5.3 that under $V_g=V_d$ condition prior to the power law stage, there is a region defined by a near saturation in the transconductance which lasts about two decades from 0.1 up to 10 seconds. The long-term power law degradation under this condition has lower values 0.18-0.21. It should be noted that degradation slopes in general are stress condition and technology dependent, and the values given here are the corresponding to Figs. 5.1-5.3. It is also observed that in general for all the stress conditions $g_m$ degradation shifts on the time scale depending upon the drain bias and the technology. For lower drain biases, the initial rise in degradation is shifted to the right on the time scale and the magnitude of the degradation is lower.

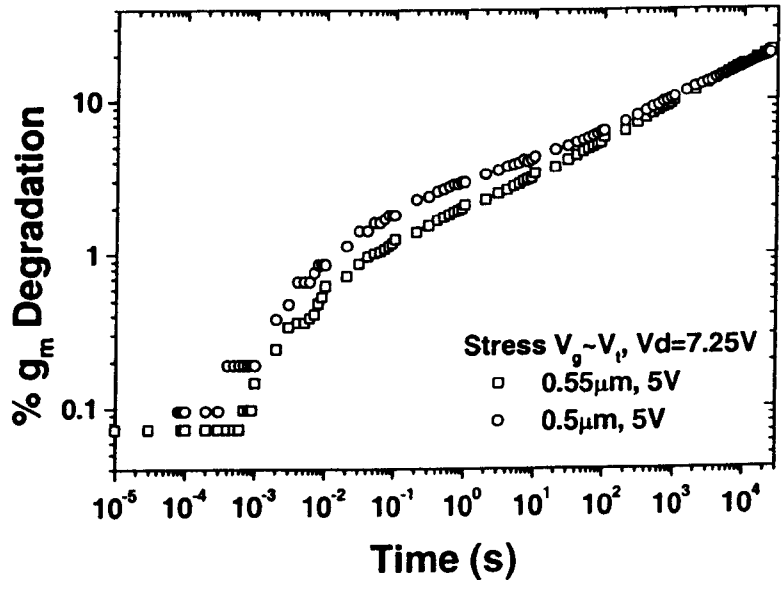


Fig. 5.2 Maximum transconductance ($g_m$) degradation behaviour for 0.55μm, 5V and 0.5μm, 5V technologies. The devices are stressed under $V_g$~$V_t$ stress conditions: ($V_d$=7.25V, $V_g$=0.7V).

### 5.2.2 Threshold Voltage ($V_t$) Degradation

In Fig. 5.4 typical degradation characteristics of threshold voltage $V_t$ for 5V technology devices are shown for different stress conditions. The threshold voltage has been obtained as an extrapolation from the linear drain current characteristics at $V_d$=0.1V from the point of maximum transconductance.

It is seen that during stage 1, there is a wide scatter in the threshold voltage data under all the bias conditions. In addition for all the stress conditions $V_t$ shifts are delayed to the onset of the power law regime, i. e. after the saturation region. The slopes of the degradation are 0.2-0.28, 0.3-0.4 and 0.2-0.3 for $V_g=V_d$, $I_{submax}$ and $V_g$~$V_t$ conditions respectively.

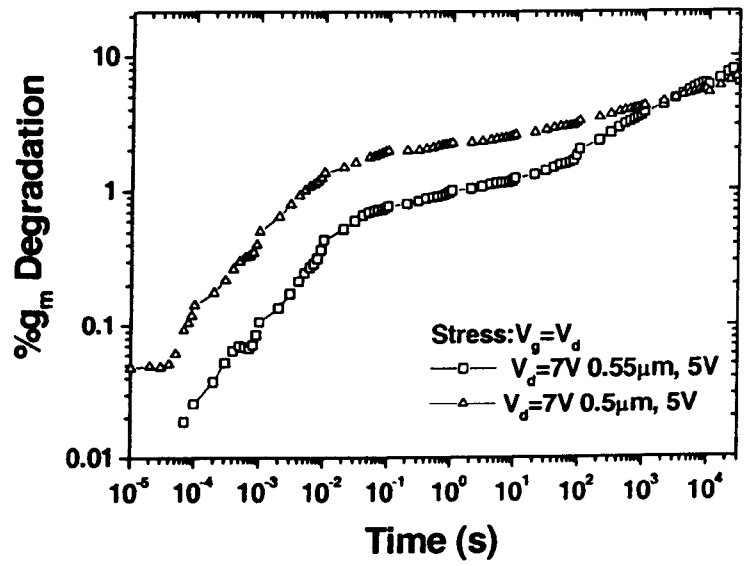


Fig. 5.3 Maximum transconductance ($g_m$) degradation behaviour for 0.55μm, 5V and 0.5μm, 5V technologies. The devices are stressed under $V_g$=$V_d$=7V stress condition.

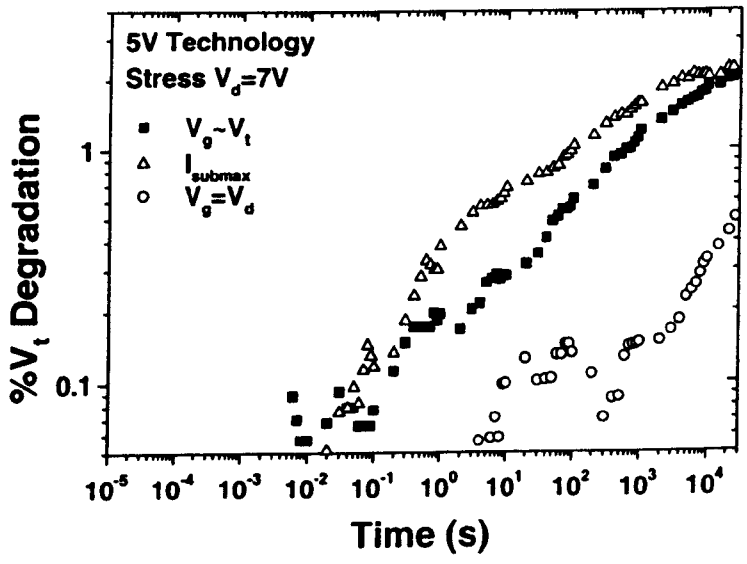


Fig. 5.4 Linearly extrapolated threshold voltage $V_t$ degradation behaviour for 0.5μm, 5V devices. The devices are stressed under $I_{submax}$, $V_g$~$V_t$ and $V_g$=$V_d$, Vd=7V stress conditions.

## 5.3 Degradation Behaviour of 3V and 2V Technologies

### 5.3.1 Transconductance ($g_m$) Degradation

For the 3V and 2V technologies, the $g_m$ degradation behaviour under the three bias conditions are shown in Figs. 5.5 and 5.6 respectively. It can be seen from Figs. 5.5 and 5.6 that the

region of early stage degradation decreases as the devices are scaled. For 3V device the duration of the early stage is much less as compared to 5V technologies. Whereas for 2V technology as seen in Fig. 5.6 the early stage degradation has almost disappeared and instead it is noted that $g_m$ degradation shows conventional power law degradation behaviour. In the long-term power law regime, the degradation slopes are 0.37-0.42, 0.21-0.36, and 0.28-0.36 for $I_{submax}$, $V_g=V_d$ and $V_g\sim V_t$ stress conditions respectively. Under $V_g=V_d$ stress condition, a smaller saturation region also exists between the rapid initial rise and the power law regime for 3V technology but is not observed for 2V technology device.

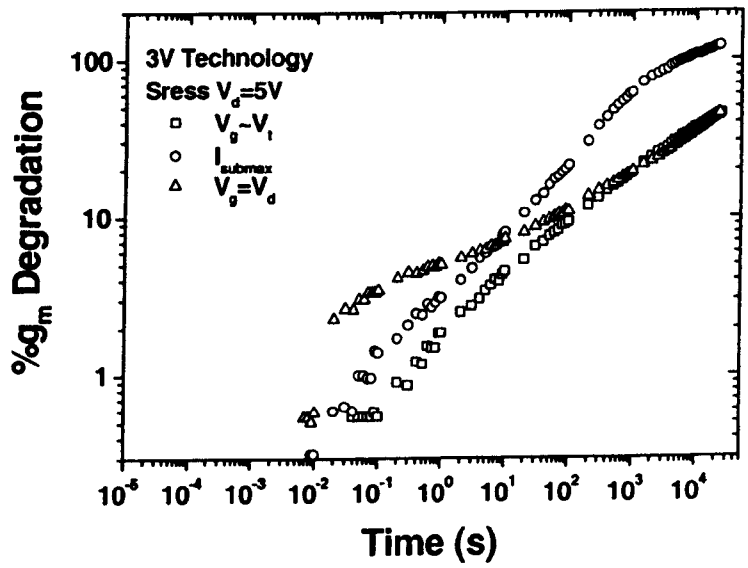


Fig. 5.5 Maximum transconductance ($g_m$) degradation behaviour for 0.36μm, 3V. The devices are stressed under stress conditions: $V_g=V_d$, $V_g=2.3V(I_{submax})$, $V_g=0.6V(V_g\sim V_t)$; $V_d=5V$.

In general, the damage in 3V and 2V devices is higher than in 5V devices as is apparent from the magnitude of the $g_m$ degradations. In addition, in contrast to 5V technologies, under worst case stress ($I_{submax}$ condition) saturation in degradation behaviour in long term stress is observed for these technologies.

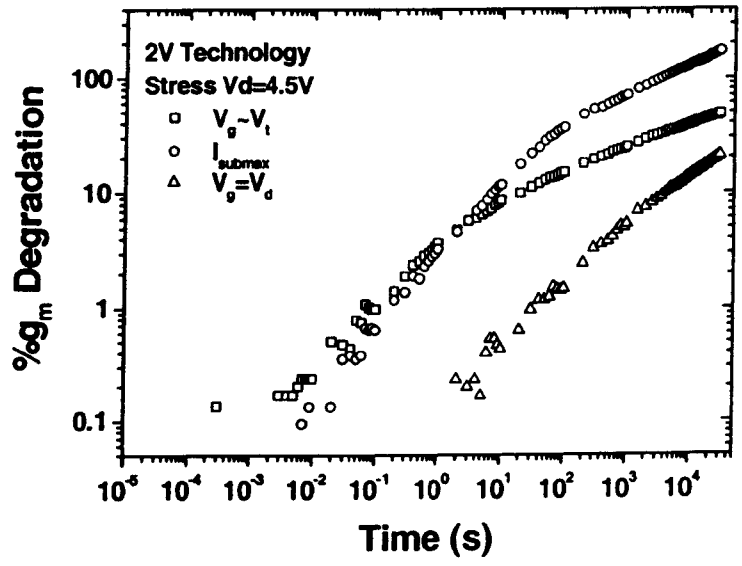


Fig. 5.6 Maximum transconductance ($g_m$) degradation behaviour for 0.32μm, 2V technology under different stress conditions. The stress biases are $V_g$=$V_d$, $V_g$=2.1V($I_{submax}$), $V_g$=0.6V($V_g$~$V_t$); $V_d$=4.5V.

### 5.3.2 Threshold Voltage ($V_t$) Degradation

In Figs. 5.7 and 5.8 the threshold voltage ($V_t$) degradation for 3V and 2V technologies is shown. The $V_t$ degradation slopes are 0.5-0.45 for 3V device and 0.6-0.65 for 2V device. An important difference between the 3V and 2V devices as compared to 5V devices is that the threshold voltage degradation is much larger in 2V and 3V technologies. In comparison to 8-10% maximum $V_t$ degradation observed for 5V technologies, for 3V and 2V technologies a much greater degradation in $V_t$ can be observed.

Further similar to $g_m$ degradation behaviour a long-term saturation of $V_t$ degradation (under $I_{submax}$ stress condition) for 2V and 3V technologies can be noticed. As the change in $V_t$ is indicative of the damage in the channel region, implying that much greater damage in the channel regions of 3V and 2V.

## 5.4 A Qualitative Model for the hot carrier degradation behaviour

As pointed in Sec. 5.1, the hot carrier degradation in LDD MOSFETs differs from $n^+$ drain MOSFETs because of the lightly doped drain and spacer oxide in the former. In LDD MOSFETs hot carrier degradation is a combination of drain series resistance increase and reduction of channel mobility [7], [12], [13], [14]. The series resistance of the device increases because the underlying silicon in the $n^-$ LDD region gets depleted due to charge

injection into the spacer oxide. This causes a reduction in the transconductance of the transistor due to a reduced current drive capability.

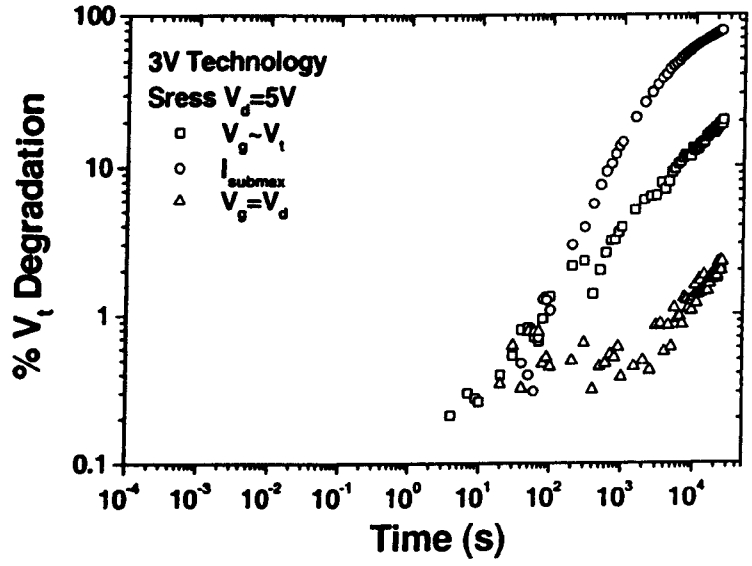


Fig 5.7 Threshold voltage degradation for 0.36μm, 3V technology under different stress conditions. The stress biases are $V_g$=$V_d$, $V_g$=2.3V($I_{submax}$), $V_g$=0.6V($V_g$~$V_t$); $V_d$=5V.

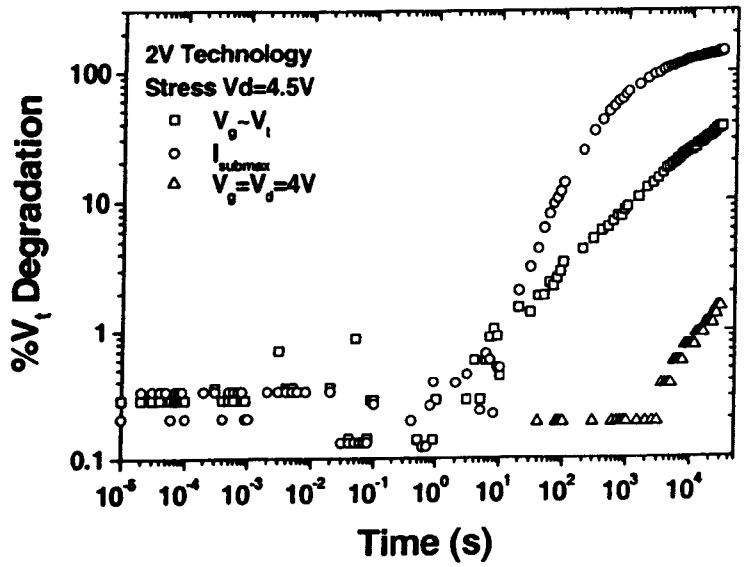


Fig 5.8 Threshold voltage degradation for 0.32μm, 2V technology under different stress conditions. The stress biases are $V_g$=$V_d$, $V_g$=2.1V($I_{submax}$), $V_g$=0.6V($V_g$~$V_t$); $V_d$=4.5V.

A model based on degradation regions shown in Fig. 5.9 can explain device degradation observed above. The early mode degradation is initiated through damage in the spacer oxide

marked Region 1 in Fig. 5.9. The quality of the oxide spacer is likely to be poorer than that of the gate oxide, and therefore this region is most likely to be degraded at the initial stages of the stress [8], [13], [15]. This leads to initial rapid degradation of $g_m$ degradation due to increase in the drain series resistance degradation. As stress time increases, the damage to the region under the gate (marked as Region 2 in Fig. 5.9) become significant and starts to degrade the channel mobility. This is indicated by change in the slope of $g_m$ degradation curves. Under long term stress, the degradation to channel mobility dominates the $g_m$ degradation whereas series resistance degradation tends to saturate.

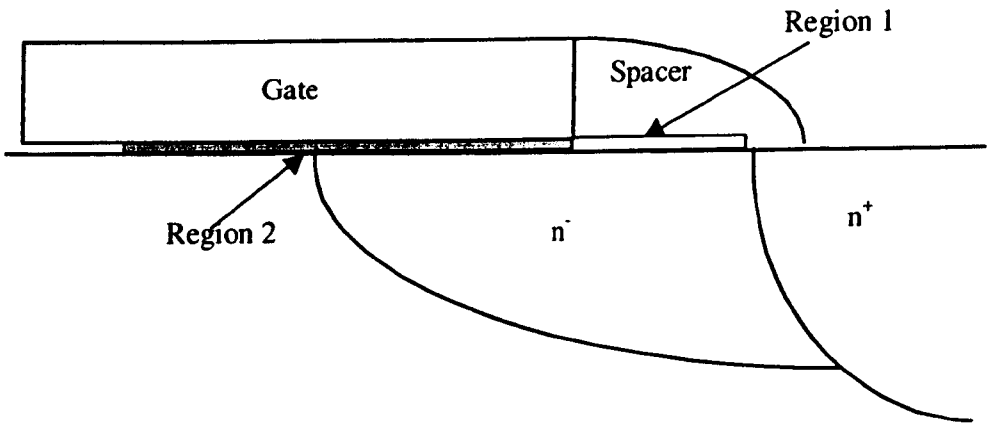


Fig. 5.9 A cross-section of LDD region showing the two damage regions.

This model of degradation is also supported by $V_t$ degradation observed for all the technologies. Since no change in $V_t$ during the early stage is observed, implies that damage during this stage is very small in the channel region*, while the damage in the spacer region does not effect $V_t$. This is due to the fact that spacer region is not under direct gate control and the effect of the damage on $V_t$ is not observed. The degradation in $V_t$ starts when the damage to channel region becomes significant.

Further, the model is also consistent with the reduction in the early stage degradation for 3V technology (Fig. 5.5) and near disappearance early stage degradation for 2V technology (Fig. 5.6). Since technology scaling is achieved by the reduction of channel length, oxide thickness, source/drain junction depth and device operating voltages [16], [17]. The reduced operating voltage enables increase in LDD doping from lightly doped to moderately doped drains (MDD) [18]. This has two consequences for hot carrier degradation behaviour. First, due to reduced device dimensions and higher drain doping, the position of the peak electric



*An additional cause of lower $V_t$ degradation has been identified as due to the screening effect of built-in drain field on the surface potential in the vicinity of the drain junction, which will be will discussed in Chapters 7 and 9.

field, which is the underlying cause of hot carrier generation, shifts from spacer region towards channel region [19], [20]. This causes more damage in channel region of the device than in spacer region. Secondly, and more importantly, as a result of increased drain doping (c. f. Table 4.1) for a fixed amount of the damage in spacer region the increase in drain series resistance will be lower for scaled devices. Therefore, both these factors contribute to a lesser increase in drain series resistance in 3V and 2V technologies as compared to that for 5V technologies. As a consequence, there is very little early stage $g_m$ degradation in 3V and 2V technologies as seen in Figs. 5.5 and 5.6. Further, as the peak electric field increases and shifts towards the channel region, there is more damage in the channel region for 3V and 2V technologies. The greater channel damage in these technologies implies more degradation in channel mobility and $g_m$ [21], [7]. This is confirmed by larger $g_m$ and $V_t$ degradation for 3V and 2V technologies as compared to 5V technologies as seen in Figs. 5.5, 5.6 for 2V and 3V technologies and Figs. 5.1-5.3 for 5V technologies.

## 5.6 Summary

In this Chapter the degradation behaviour of experimentally measured parameters $g_m$ and $V_t$ of different generations of graded drain technologies beginning from stress time in microseconds is studied. Early stage degradation behaviour, deviating from conventionally observed power law, with characteristics dependent on a particular technology is reported. For 5V technologies a clear early stage lasting about 100ms is observed, whereas the extent of the early stage is reduced significantly for 3V technology while it disappears for 2V technology. A qualitative model based on drain series resistance degradation due to damage in the spacer region the early stage and mobility degradation due to damage in the channel and the gate drain-overlap region is used to explain the results. These results give an important insight into the early stage evolution of hot carrier damage of the different technology generations. These findings highlight the importance of studying the spacer and channel degradation and their relative contribution in determining the device degradation behaviour, which is the focus of the study in the remainder of this thesis.

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# CHAPTER 6

# ANALYSIS OF DEGRADATION OF 5V TECHNOLOGIES

## 6.1 Introduction

The mechanisms of device degradation in MOSFETs due to hot carriers are of considerable interest to semiconductor industry. It is well known that large electric fields at the drain junction generate hot carriers, leading to localized damage in the oxide and at the Si-SiO2 interface. In order to reduce hot carrier effects, Lightly Doped Drains (LDD) are employed to replace conventional $n^+$ drain in MOSFETs [1]. However, LDD MOSFETs suffer from additional degradation mechanisms associated with the spacer oxide, whereby the hot carrier damage in the spacer oxide by interface state creation and/or negative trapped charge can deplete the underlying lightly doped $n^-$ region [2]. This leads to an increase in the drain series resistance and degradation in device current carrying capability. On the other hand, the damage in the channel region leads to the carrier mobility degradation due to Coulombic scattering by trapped charge at and near the interface as in the case of conventional devices [3]. Long term hot carrier degradation of LDD MOSFETs has been widely reported, but not much work has been done to study the d. c. degradation behaviour for short stress time scales (early stage). Studying early stage degradation behaviour is important, since under normal operation it is likely that the device will suffer from this type of damage within very short span of operation. Further for LDD MOSFETs, understanding the mechanisms of hot carrier degradation in the oxide spacer region of LDD MOSFETs is an important aspect of device reliability and process design. In this regard the work presented in Chapter 4 using stress time of microseconds in sub-micron LDD n-MOSFETs showed a unique early stage deviation from the power law behaviour, clearly identifying the damage in the spacer. A qualitative model based on series resistance and the mobility degradation was put forward as an explanation of the degradation behaviour of these technologies.

In this chapter a detailed analysis of 5V technologies is presented which supports the degradation model proposed. The damage is first analysed by series resistance and the mobility degradation extraction methodology, which is developed in this work, based on L-array method using Moneda technique [4]. The evolution of hot carrier degradation of these

technologies is presented for different stress conditions, namely maximum electron injection ($V_g$=$V_d$), maximum substrate current ($I_{submax}$) and maximum hole injection ($V_g$~$V_t$). The degradation of the drain series resistance and mobility is interpreted using separate models for inversion and accumulation layer mobilities. This method allows a quantitative estimation of the drain series resistance increase from very short stress time scales and an evaluation of its impact on other device parameters such as transconductance. Further the magnitude of the drain series resistance degradation determined using this approach can be used in device lifetime prediction [5].

It is shown that series resistance degradation shows a two stage saturating feature, with the early stage lasting until 100ms. The mobility degradation is shown to dominate under long term degradation while series resistance degradation tends to saturate. The nature of hot carrier degradation in the early stage under the three stress conditions ($V_g$=$V_d$, $I_{submax}$ and $V_g$~$V_t$) is investigated using alternate stress experiments and charge pumping measurements. By measuring increase in charge pumping current, interface state generation in the spacer region is investigated. Studying a correlation between extracted series resistance and interface state generation identifies the relative roles of interface state generation and trapping. It is seen that only under $V_g$=$V_d$ condition a part of the damage is contributed by trapping mechanism, while interface state generation is seen to be dominant cause of degradation under the other two stress conditions. Further the causes of saturating series resistance behaviour under the different stress conditions are discussed.

## 6.2 An Extraction Methodology for Series Resistance and Mobility Degrdation

It is well established that degradation of an LDD MOSFET is caused both by the damage to the spacer region and channel region [2], [5], [6]. In order to accurately quantify the relative roles of the two degradation mechanisms on overall device degradation an extraction methodology is developed in this work. This method is based on L-array technique proposed by Moneda et. al. [4].

The linear on resistance of the device is given by the sum of the channel resistance ($R_{Chan}$) and the source/drain series resistance ($R_{SD}$)

$$R_{ON} = R_{Chan}(V_{gs}) + R_{SD}(V_{gs}) \tag{6.1}$$

Incorporating the gate voltage modulated $n^-$ region resistance [7], [8] under high gate voltage overdrive, $R_{ON}$ can be expressed as,

$$R_{ON} = \frac{L_{eff}}{\mu_{eff} C_{OX} W(V_{gs} - V_t - \alpha V_{ds})} + \frac{\Delta L}{\mu_{eff,acc} C_{OX} W(V_{gs} - V_{FB})} + R_{SD} \qquad (6.2)$$

where $L_{eff} = L_{drawn} - \Delta L$, $\Delta L$ is equal to the gate drain and source region overlap, $V_{FB}$ is the average flat band voltage for the gate controlled $n^-$ region, $\mu_{eff}$ and $\mu_{eff,acc}$ are the effective electron mobilities in the channel inversion layer and accumulation layers in the gate and LDD overlap regions respectively. $R_{SD}$ is the resistance of the rest of the ohmic LDD region including the contact resistance, and is equal to the sum of the source and drain series resistance ($R_{SD} = R_S + R_D$), $\alpha$ is the body effect parameter, other parameters have their usual meanings. It should be mentioned that $R_{SD}$ is also modulated weakly by the gate voltage through fringing field, but this dependence can be ignored for the hot carrier degradation studies.

A number of models exist for effective inversion layer mobility $\mu_{eff}$ as a function of the gate voltage resulting from the effect of the vertical electric field [9]. However, the conventional well known universal relation proposed in [10] is a good choice as a first order approximation, to model the behaviour with reasonable accuracy. Further it has been shown experimentally [11], that the accumulation and inversion layer mobilities show a similar universal behaviour at large effective fields, which correspond to a strongly inverted channel. Therefore the gate voltage dependence of the accumulation layer mobility has a similar functional dependence as that of the inversion layer mobility, if the expression for calculating effective surface field is modified accordingly. Hence, the first order effective inversion and accumulation layer mobilities can be modelled as

$$\mu_{eff} = \frac{\mu_0}{1 + \theta(V_{gs} - V_t)} \qquad (6.3)$$

$$\mu_{eff,acc} = \frac{\mu_0}{1 + \theta V_{gs}} \qquad (6.4)$$

Substituting $\beta = \mu C_{ox} W/L$ and substituting (6.3) and (6.4) in (6.2) after algebraic manipulation yields

$$R_{ON} = \frac{1}{\beta}\left[1 + \frac{1+\theta V_{FB}}{r[1+\delta(V_{gs})]}\right]\frac{1}{(V_{gs} - V_t - \alpha V_{ds})} + \frac{\theta}{\beta}\left[1 + \frac{1}{r}\right] + R_{SD} \qquad (6.5)$$

where

$$\delta(V_{gs}) = \left(\frac{V_t - V_{FB} + \alpha V_{ds}}{V_{gs} - V_t - \alpha V_{ds}}\right) \text{ and } r = L_{eff}/\Delta L \qquad (6.6)$$

A regression of $R_{ON}$ vs $1/(V_{gs}-V_t-\alpha V_{ds})$ has a slope, m, which depends on $V_{gs}$ through the term $\delta(V_{gs})$, and intercept $R_{int}$ which also has a weak $V_{gs}$ dependence through the gate fringing field modulation of $R_{SD}$. The term $\theta V_{FB} << 1$, as $\theta$~0.08-0.1 for the MOSFETs under study, therefore it can be safely neglected. Also, for measurements in linear region $V_{ds} \leq 0.1$ and value of $\alpha$ is about 0.6 making the term $\alpha V_{ds} \leq 0.06$. For $(V_{gs} - V_t) \geq 1$ and for typical values of $(V_t - V_{FB}) < 1$, the term $\delta(V_{gs}) \leq 1$. It is also notable that a +/- 10% variation in $V_t$ or $V_{FB}$ due to hot carrier injection, which is the worst case condition for the devices within the examined range, does not affect the preceding approximations significantly. Therefore, taking upper bound for the second term in first square brackets in equation (6.5) as:

$$\left[1 + \frac{1+\theta V_{FB}}{r[1+\delta(V_{gs})]}\right] = \left[1 + \frac{1}{r}\right] \qquad (6.7)$$

by ignoring the terms $\delta(V_{gs})$ and $\theta V_{FB}$, and neglecting any dependence of $R_{SD}$ on $V_{gs}$, equation (6.5) can be generalised as

$$R_{ON} = \frac{1}{\beta}\gamma\frac{1}{(V_{gs} - V_t - \alpha V_{ds})} + \frac{\theta}{\beta}\gamma + R_{SD} \qquad (6.8)$$

where

$$\gamma = 1 + \frac{1}{L_{eff}/\Delta L} \qquad (6.9)$$

is approximately equal to 1.26 for the devices under study. $R_{ON}$ in equation (6.8) can be interpreted as the sum of channel resistance of two MOSFETs with current drive parameters $\beta$ and $(L_{eff}/\Delta L)\beta$, and the ohmic resistance of LDD regions, $R_{SD}$. It should be emphasised that

equation (6.8) is strictly valid under strong inversion conditions where electron inversion and accumulation layer mobility have similar effective field dependence.

By using equation (6.8) for $R_{ON}$, the drain current in linear region can be found from $I_{DS}=V_{ds}/R_{ON}$, giving

$$I_{DS} = \frac{\beta(V_{gs} - V_t - \alpha V_{ds})V_{ds}}{\gamma[1+\theta(V_{gs} - V_t - \alpha V_{ds})]+\beta R_{SD}(V_{gs} - V_t - \alpha V_{ds})} \tag{6.10}$$

The linear regression of (6.8) gives for slope and intercept respectively,

$$m = \gamma\frac{1}{\beta} \tag{6.11}$$

$$R_{int} = \gamma\frac{\theta}{\beta} + R_{SD} \tag{6.12}$$

Based on (6.2), (6.11) and (6.12), the degradation of $R_{SD}$ corresponds to the damage created in the spacer region, and the degradation in slope m corresponds to the mobility degradation indicating the damage in the gate-drain overlap/channel regions. The changes in $R_{SD}$ correspond to changes in the drain series resistance $R_D$ ($\Delta R_{SD}=\Delta R_D$), since the damage is restricted to the drain junction. The degradation in parameter $\beta$ is affected by the degradation of the accumulation layer mobility in the gate drain LDD overlap region and the inversion layer mobility in the channel region.

From (6.11) and (6.12) for unstressed devices differing only in the drawn gate lengths, a plot of m v/s. L yields $\Delta L$, whereas a plot of $R_{int}$ v/s (L - $\Delta L$) gives $\theta$ and $R_{SD}$. After devices are subjected to hot carrier stress, both $\beta$ and $R_{int}$ are found from equation (6.8). The degradation in parameter $\beta$ is caused by the channel mobility $\mu$ with some contribution from $C_{OX}$. In the extraction of $R_{SD}$ from equation (6.12), it is assumed that the parameter $\theta$ does not change significantly after hot carrier stress as a result of charge created in the oxide. This assumption is verified later by showing that the calculated and measured $g_m$ values match to a good accuracy, after stress using $\theta$ obtained for unstressed devices.

Differentiating equation (10) with respect to $V_{gs}$ gives transconductance, $g_m$,

$$g_m = \frac{\beta\gamma V_{ds}}{[\gamma(1+\theta(V_{gs}-V_t-\alpha V_{ds}))+\beta R_{SD}(V_{gs}-V_t-\alpha V_{ds})]^2} \tag{6.13}$$

The percentage degradation in $g_m$ with respect to that of an unstressed device, using (6.13), after stress time t can be expressed as

$$\Delta g_m(t) = 1 - \frac{\beta(t)}{\beta(0)}\left[\frac{\gamma[1+\theta(V_{gs}-V_t(0)-\alpha V_{ds})]+\beta(0)R_{SD}(0)(V_{gs}-V_t(0)-\alpha V_{ds})}{\gamma[1+\theta(V_{gs}-V_t(t)-\alpha V_{ds})]+\beta(t)R_{SD}(t)(V_{gs}-V_t(t)-\alpha V_{ds})}\right]^2 \tag{6.14}$$

where zero and t in parentheses denote initial values and values at time t respectively.

The hot carrier degradation of the measured $g_m$ (found as the maximum slope of $I_{ds}$-$V_{gs}$ curves), and extracted parameters $R_{SD}$ and $\beta$ are studied as a function of time and different stress conditions beginning with very short stress time. The $g_m$ degradation values predicted by equation (6.14) are compared with the measured values, obtained directly from $I_{ds}$-$V_{gs}$ curves, and are shown to be in good agreement, validating the models and approximations used.

## 6.3 Drain Series Resistance and Mobility Degradation

The analysis of the $g_m$ degradation behaviour has been carried out by extracting the series resistance ($R_D$) and mobility ($\beta$) using the methodology described in Sec. 6.2. As was pointed out, this technique enables separation of the damage in the spacer region from that in the gate-drain overlap and channel regions.

In Fig. 6.1, 6.2 and 6.3 the degradation behaviour of extracted $R_D$ and $\beta$ (which represents the mobility, $\mu$, degradation) along with measured $g_m$ degradation are shown for devices stressed under $V_g=V_t$, $I_{submax}$ and $V_g=V_d$ conditions. For all the stress conditions a two stage $R_D$ degradation is clearly noticed. A sharp degradation in the early (first) stage, which lasts up to 100ms can be seen. From Figs. 6.1, 6.2 and 6.3, it can be seen that the $g_m$ degradation can be split into two components: a) degradation in the series resistance ($R_D$) due to the damage in the spacer oxide in the early stage, and b) degradation in electron mobility ($\beta$) due to the damage in $n^-$ LDD overlap region and channel region dominating at long stress time.

The initial slope of $R_D$ degradation lies between 0.45-0.55. In the second regime, the slope is 0.15-0.18 under $V_g \sim V_t$ and $I_{submax}$ condition, which agrees well with that reported by Walter et al [12]. Under $V_g=V_d$ condition however, the slope is 0.05-0.07 and accounts for the observed saturation in $g_m$ degradation in the second stage (Fig. 6.3). A small degradation in $R_D$ under $V_g=V_d$ condition after about 100 seconds is also noticeable but this degradation does not significantly affect $g_m$ which has begun to be dominated by the mobility degradation by this time. It is observed that under $V_g=V_d$ condition the mobility degradation is delayed in comparison to $V_g \sim V_t$ and $I_{submax}$ conditions. Further, the results of the $R_D$ and mobility degradation support negligible threshold voltage $V_t$ shifts observed during the early stage (Fig. 5.4), as the majority of the damage in the early stage is located in the spacer oxide outside the region of the gate control.

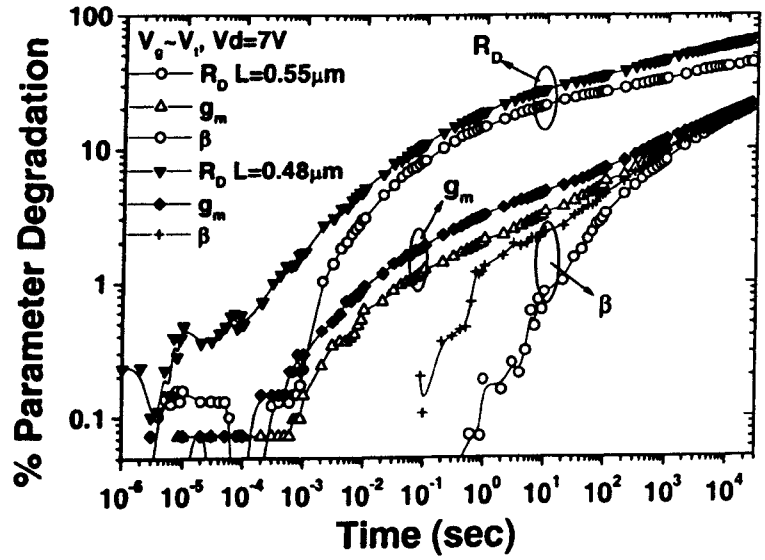


Fig. 6.1 Time dependence of the extracted drain series resistance $R_D$ and mobility (β) degradation along with experimental $g_m$ degradation under $V_g \sim V_t$ stress condition, $V_d$=7V for 5V technologies, L=0.55 and 0.48μm.

The $g_m$ degradation observed under $V_g \sim V_t$ stress condition is consistent with results reported in [13]-[16]. It has been shown that under $V_g \sim V_t$ stress, as a result of hole injection three different types of damages are generated: hole trapping, interface traps and neutral electron traps [17], [18]. While the hole trapping near the drain junction can lead to $g_m$ enhancement due to channel shortening effect of the trapped holes [17], [18], in certain cases (including the present) the net $g_m$ degradation is determined by overall effect of trapped charge and interface

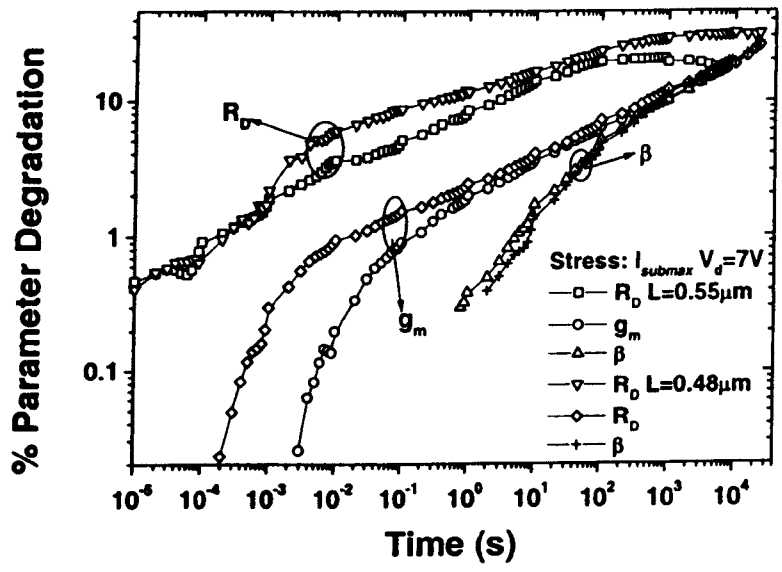


Fig. 6.2 Time dependence of the extracted drain series resistance $R_D$ and mobility (β) degradation along with experimental $g_m$ degradation under $I_{submax}$ stress condition, $V_d$=7V for 5V technologies, L=0.55 and 0.48μm.

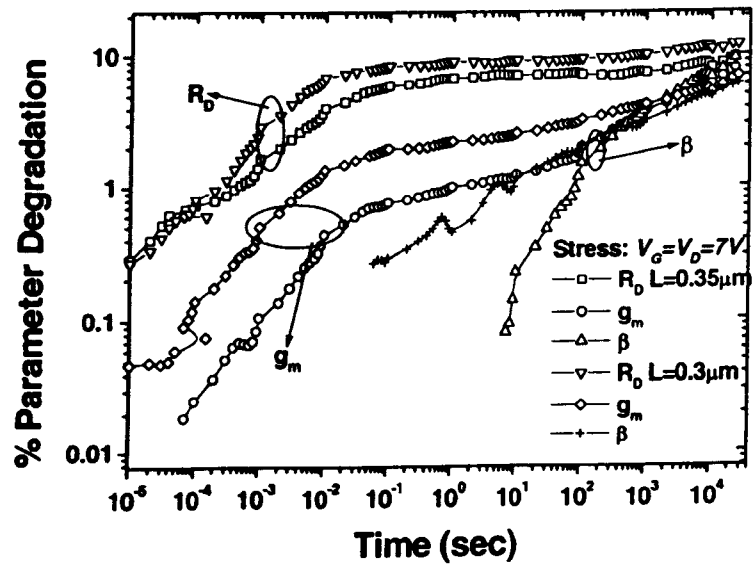


Fig. 6.3 Time dependence of the extracted drain series resistance $R_D$ and mobility (β) degradation along with experimental gm degradation under $V_g$=$V_d$=7V stress condition, for 5V technologies, L=0.55 and 0.48μm.

states [16], [17], [19], [20]. The relative dominance of trapping over interface state creation will depend in general on processing conditions, oxide quality and the position of trapped charge and generated interface states. The $g_m$ degradation observed here under $V_g$~$V_t$ stress

(even under $V_g(=0.4V)<V_t$) is the result of dominant effect of interface states over trapping, this effect will be further demonstrated in Sec. 6.5 below using charge pumping and alternate stress experiments. This could be attributed to lesser number of oxide traps present in the oxide layer for the devices investigated in this study.

## 6.4 Verification

The extraction procedure developed for the series resistance and mobility degradation is verified by comparing measured $g_m$ degradation obtained directly from $I_{ds}$-$V_{gs}$ characteristics with that calculated by equation (6.14). The results of the measured and calculated $g_m$ degradations under $V_g \sim V_t$, $I_{submax}$ and $V_g=V_d$ stress condition are shown in Figs. 6.4, 6.5 and 6.6 respectively. It is noted that in general a good match is obtained between measured and calculated values. The calculated values exceed measured values by maximum of about 10%, and the degradation in calculated and measured values fit to within 10% variation.

This variation could be the result of a number of factors: simple model used for the universal mobility behaviour, the mobility degradation due to lateral field not being taken into account and other simplifying assumptions made while deriving equation (6.14). But more importantly, the trend in the degradation behaviour in the calculated and measured values is reproduced to a good accuracy, which validates the parameter extraction procedure and justifies the assumptions and models used.

## 6.5 Nature of Hot Carrier Degradation in Early Stage

It is well known that the type of carrier involved in hot carrier degradation depends on the stress bias conditions [21], [22]. Holes are predominantly injected under $V_g \sim V_t$ condition, both electrons and holes under $I_{submax}$ conditions, whereas electrons are predominantly injected under $V_g=V_d$ condition. The damage due to hole injection can result in either hole trapping creating positive charge or creation of interface states [14], [17]. Of these two mechanisms, only the creation of acceptor type interface states can lead to $R_D$ increase under $V_g \sim V_t$ (since the trapping of positive charge would create accumulation layer in the LDD).

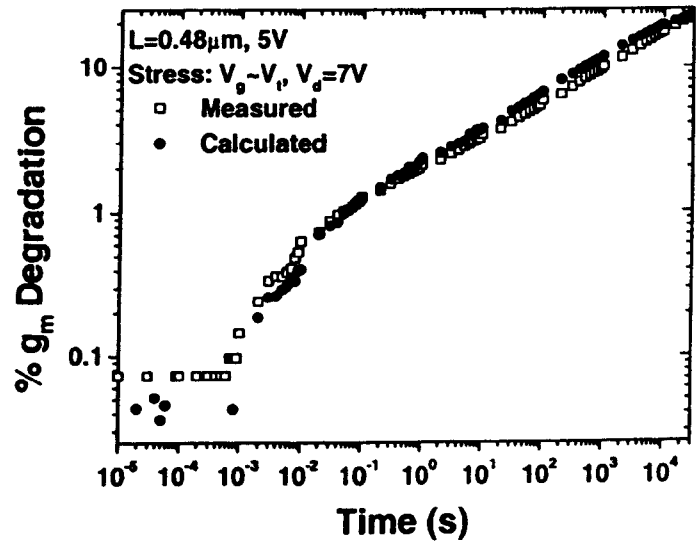


Fig. 6.4 A comparison of measured and calculated values of $g_m$ degradation (using equation (6.14)) under $V_g$~$V_t$ stress condition, $V_d$=7V. The results are shown for L=0.48, 5V technology device.

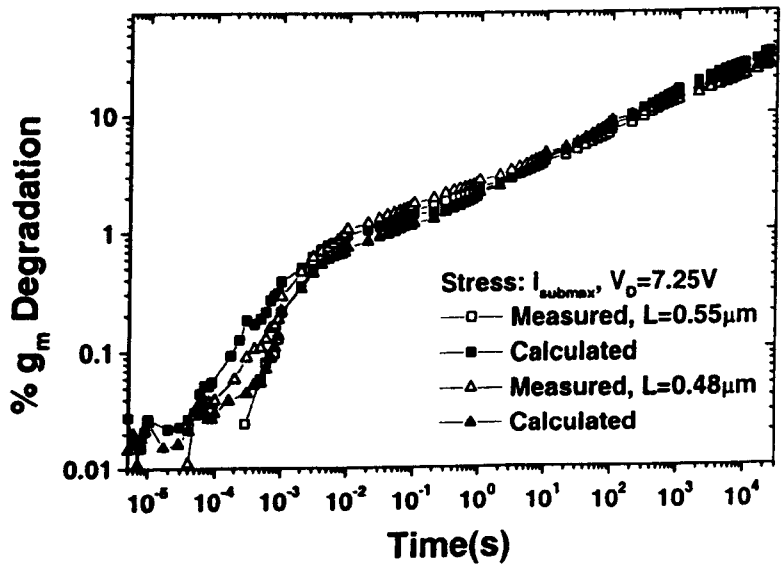


Fig. 6.5 Results of measured and calculated values of $g_m$ degradation (using equation (6.14)) under $I_{submax}$ stress condition, $V_d$=7V. The results are shown for L=0.55 and 0.48, 5V technology devices.

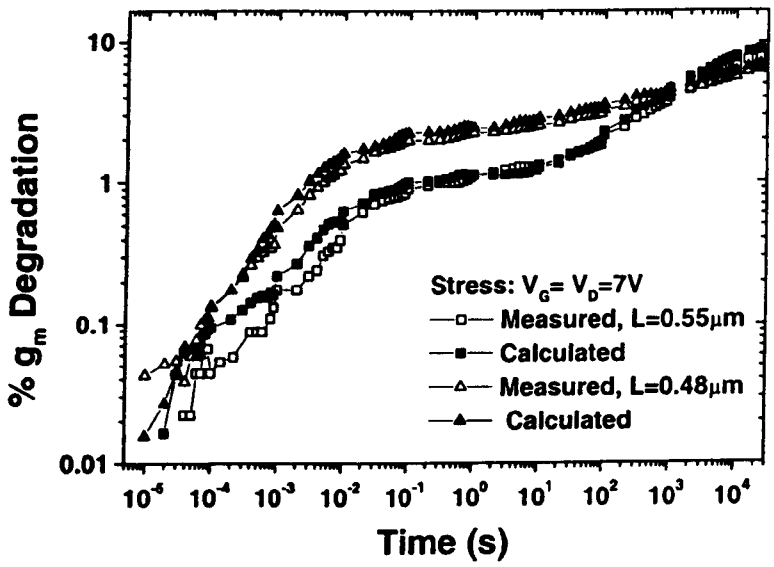


Fig. 6.6 Results of measured and calculated values of $g_m$ degradation (using equation (6.14)) under $V_g$=$V_d$=7V stress condition. The results are shown for L=0.55 and 0.48, 5V technology devices.

In experiment, since $R_D$ degradation is observed under $V_g$~$V_t$ (Fig. 6.1) stress condition, this implies that hole trapping is not a dominant degradation mechanism in the spacer oxide. The $R_D$ degradation under $I_{submax}$ condition also points to the damage by interface state creation, as this mechanism is well known to occur under this condition [17], [23]. However, the nature of degradation in the early stage under $V_g$=$V_d$ condition is not evident, it could be either due to electron trapping or interface state creation.

It has been reported that the hot carrier damage under $V_g$=$V_d$ is dominated by electron trapping [17], [18]. Therefore, it would appear that $R_D$ degradation in the early stage for this condition is also by electron trapping. However, on the other hand, from Figs. 6.1-6.3, it is seen that the degradation slopes, magnitudes and duration of early stage are very similar for all the three stress conditions. This supports the argument that degradation in early stage for all conditions is predominantly by interface state creation. To further clarify this issue and establish the dominant degradation mechanism in the early stage, two types of experiments are performed. The first of these experiments involves alternate electron-hole injection [18] and in the second set charge pumping ($I_{cp}$) measurements after every stress cycle. While the alternate electron-hole injection experiments can be used to quantify the role of trapping, the charge pumping measurements can explicitly provide evidence of the damage by interface state creation.

### 6.5.1 Alternate Stress Experiments

In these experiments, stress and measurement cycles are performed under $V_g=V_d=7.25V$ condition followed by similar cycles under $V_g \sim V_t$, $V_d=7.25V$ for the same stress period as the proceeding stress cycle under $V_g=V_d$. The stress time is applied on log scale and time on x-axis is the total stress time including that of all the preceding cycles. Fig. 6.7 shows result of the $g_m$ degradation obtained under these conditions.

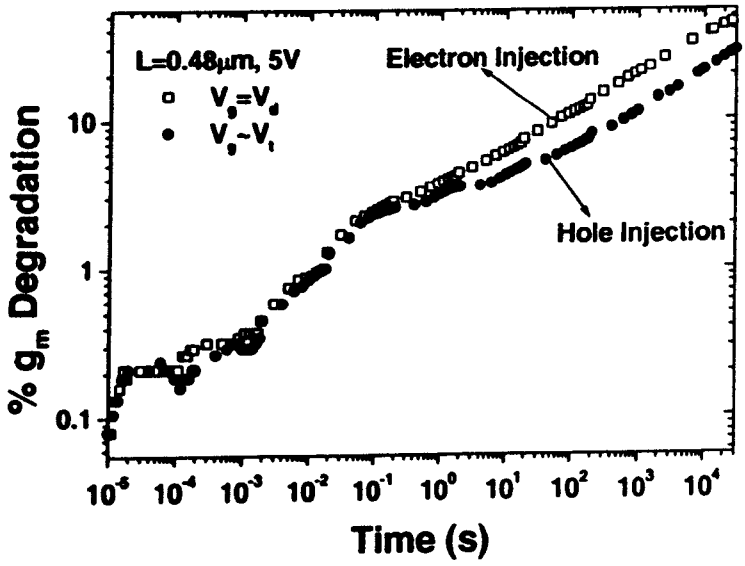


Fig. 6.7 The results of $g_m$ degradation behaviour under alternate injection for $V_g=V_d=7.25V$ and $V_g \sim V_t$, $V_d=7.25V$ stress conditions. Each stress and measurement cycle under $V_g=V_d$ condition is followed by stress and measurement cycle under $V_g \sim V_t$ condition. The stress cycle is started with stress under $V_g=V_d$ condition, the time on x-axis is combined total stress time of stress under $V_g=V_d$ and $V_g=V_t$ stress conditions.

If trapping were the cause of degradation under $V_g=V_d$ condition in the early stage, then hole injection under $V_g \sim V_t$ condition would lead to neutralisation of trapped electrons with holes, which would result in a recovery of $g_m$ degradation. From Fig. 6.7 no significant neutralisation and recovery in $g_m$ degradation during first 1ms of the early stage is seen. Between 1ms-100ms a recovery in $g_m$ degradation is noted which could be attributed to component of electron trapping during this stage.

A significant recovery in $g_m$ degradation is observed as shown in Fig. 6.8 only after the device is stressed under $V_g=V_d$ stress condition for long (more than 1000 seconds) stress time. This happens when sufficient electron trapping has occurred in the gate oxide under long term stress to allow a significant recovery in $g_m$ degradation in subsequent stress cycle

under $V_g$~$V_t$ stress. It is also noted in Fig. 6.8 that under $V_g$~$V_t$ stress condition after neutralisation (about 500 seconds) has occurred, the $g_m$ starts to degrade again as a result of dominance of interface state creation. This shows that holes injected under $V_g$~$V_t$ stress condition play a dominant role in interface state creation in comparison to trapping.

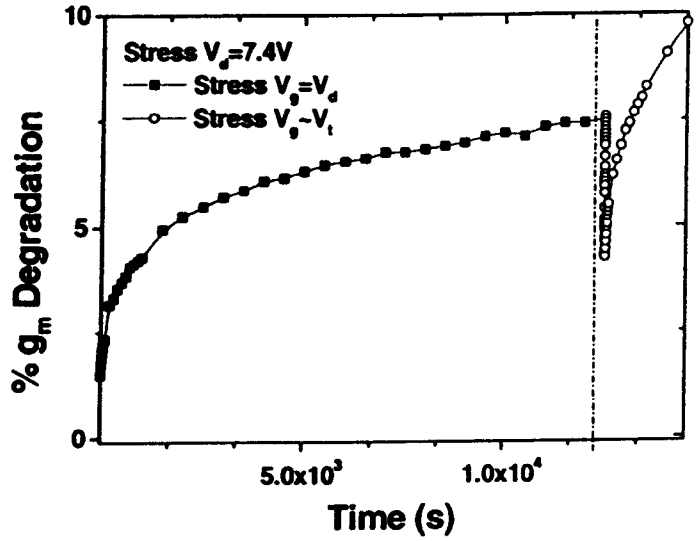


Fig. 6.8 Results of $g_m$ degradation for L=0.48μm, 5V device first stressed under $V_g$=$V_d$ condition for 12500 seconds, followed by stress under $V_g$~$V_t$ for 2000 seconds, the drain stress voltage is 7.4V.

Further, from Fig. 6.7 it is noted that the saturation observed upto 10 seconds under $V_g$=$V_d$ condition disappears under alternate injection experiments, and instead an enhanced $g_m$ degradation is observed after the electron injection stress cycle under $V_g$=$V_d$ condition. The disappearance of saturation for alternate stress experiments can be explained by the fact that the degradation is now dominated by interface state creation under $V_g$~$V_t$ cycles. The enhanced degradation observed, after early stage, for stress under $V_g$=$V_d$ cycle in Fig. 6.7 can be attributed to neutralisation of trapped holes and the filling of the neutral electron traps created in the oxide during previous hole injection cycle [24]. The recovery in $g_m$ degradation after stress cycle under $V_g$~$V_t$ condition is due to neutralisation of electrons trapped in the gate oxide during preceding stress cycle under $V_g$=$V_d$ condition by injected holes.

### 6.5.2 Charge Pumping Measurements

In the charge pumping measurements, the devices are stressed and $I_{ds}$-$V_{gs}$ measurements are done for the three stress conditions as before, and after each stress period constant base

charge pumping is performed as discussed in Chapter 4 Sec. 4.5.2.3 [25], [26]. The gate of the device is connected to a pulse generator (HP8116A), and the source and drain are grounded, while substrate charge pumping ($I_{cp}$) current is measured. A series of gate pulses of frequency 100kHz is applied to the gate, with the base of the gate pulse ($V_{gl}$) held constant while high level ($V_{gh}$) is swept. Under this arrangement the effective charge pumping length is determined by two points along the device whose flatband voltage is greater than or equal to $V_{gl}$ and threshold voltage is less or equal to $V_{gh}$ (c. f. Fig. 4.7) [27]. By keeping $V_{gl}$ fixed at sufficiently low value and varying $V_{gh}$, the effective length of the device interface contributing to charge pumping area is swept from deep in the drain/source region of the device whose flatband voltage is $V_{gl}$, to the middle of the channel where whole of the device contributes to charge pumping. When $V_{gh}$ reaches threshold voltage corresponding to the channel the charge pumping current saturates. For any value of $V_{gh}$, the charge pumping current, $I_{cp}$, is given by (4.6)

$$I_{cp} = qfW\delta LN_{it} \tag{6.15}$$

where q is electronic charge, f is the gate pulse frequency, W is device width, $\delta L$ is the length of the interface region contributing to charge pumping current. From the increase in charge pumping current at $V_{gh}$ level less than the local threshold voltage at the gate edge, the amount of interface states created in the spacer region can be directly determined using (6.15)

$$\Delta N_{it} = \Delta I_{cp}/(qfW\delta L/2) \tag{6.16}$$

where $\Delta N_{it}$ is the increase in interface states after stress and factor $\delta L/2$ in the denominator accounts for the fact that the damage occurs only in the drain region.

In the experiments the increase in $I_{cp}$ current for different $V_{gh}$ values lower than threshold voltage at the gate edge (which was determined from simulations to be about −1.2V) is compared with the corresponding $R_D$ degradation. The value of $V_{gl}$ for the measurements was fixed at −8V. Fig. 6.9(a) shows under $V_g \sim V_t$, $I_{submax}$ and $V_g = V_d$ stress conditions the increase in constant base charge pumping current for $V_{gh}$ levels correlating very closely with corresponding $R_D$ degradation in Fig. 6.9 (b). This implies that $I_{cp}$ increase in Fig. 6.9(a) is due to interface states created in the spacer region.

The acceptor like states below the Fermi level in the n-LDD region will get negatively charged by acquiring electrons, leading to the depletion of the LDD region, and therefore to an increase in $R_D$. It is postulated that these states are distributed in a Gaussian type profile, with a peak around the middle of the band-gap [29], as shown in Fig. 6.10. Thus, when the interface is negatively charged, the energy bands will be bend upwards, leading to the de-trapping of part of the interface states. However, it is argued that with the increase in stress time, the density of the interface traps will also increase proportionately, so that there is a significant fraction of interface states below Fermi level to create the negative charge, as shown in Fig. 6.10, leading to a continuous increase in the $R_D$.

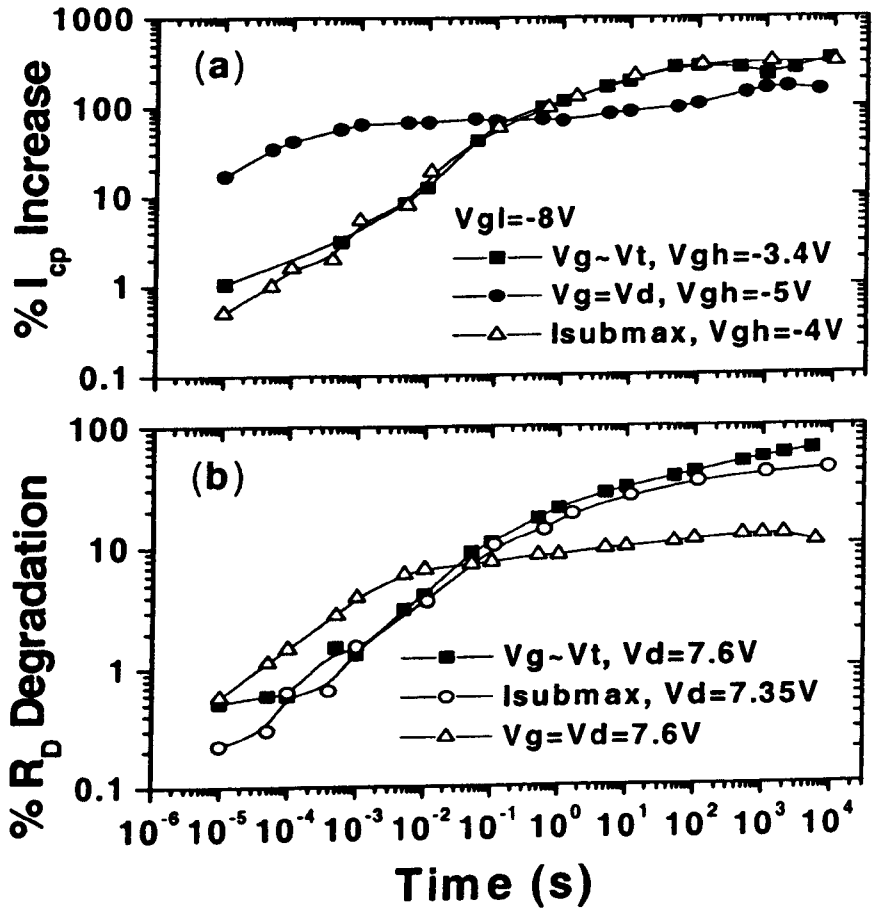


Fig. 6.9 (a) Increase in charge pumping current ($I_{cp}$) under $I_{submax}$, $V_d$=7.35V, $V_g$=$V_d$=7.6V and $V_g$~$V_t$, $V_d$=7.6V stress conditions, (b) Increase in the drain series resistance ($R_D$) for the devices in Fig. 6.9(a).

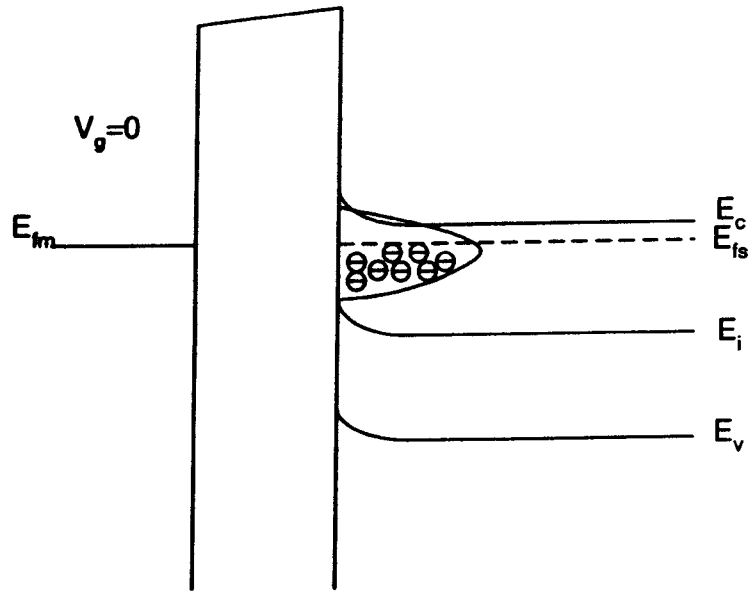


Fig. 6.10 Schematically shows the distribution and occupancy of the acceptor-like states, in the upper half of the bandgap, generated in the spacer region after hot carrier stress.

It is seen from Fig. 6.9(a) that negative $V_{gh}$ level for which $I_{cp}$ increase correlates with $R_D$ is largest under $V_g$=$V_d$ stress condition and lowest under $V_g$~$V_t$ stress condition. This indicates that, under $V_g$=$V_d$ stress condition the damage occurs farthest into the spacer region from the gate edge while it is closest to the gate edge under $V_g$~$V_t$ stress condition. This conclusion is also confirmed by simulated electric field for the devices studied in the experiments. The 2D device simulator MEDICI [28] with energy balance module is used. Fig. 6.11 shows lateral electric field profiles for the drain voltage fixed at 7V and the gate voltages emulating different injection region from $V_g$~$V_t$ through $I_{submax}$ to $V_g$=$V_d$. From Fig. 6.11 it is seen that, for fixed drain voltage, as the gate voltage is increased the location of peak electric field shifts to right into the spacer region due to the effect of vertical field. Thus the region of maximum hot carrier generation shift to deeper into the spacer region as the gate voltage is increased confirming results of Fig. 6.9(a).

The $N_{it}$ generation under $V_g$~$V_t$ and $I_{submax}$ stress conditions seen in Fig. 6.9(a) shows two stage time-saturating characteristics. Under $V_g$=$V_d$ stress condition it can be seen that after early stage a saturation between 0.01-10 seconds followed by $N_{it}$ generation in the second stage with much lower rate. The long term saturating $N_{it}$ generation characteristics under $V_g$~$V_t$ and $I_{submax}$ condition can be attributed to finite number of defect precursors in the spacer region [29].

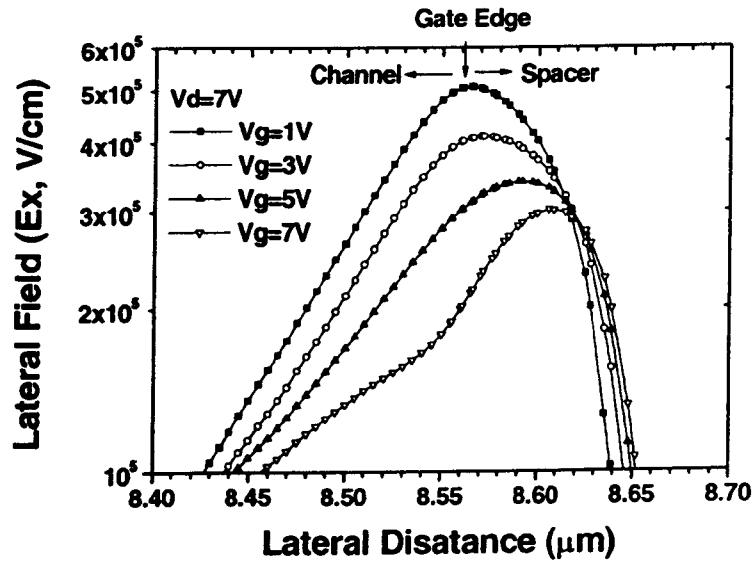


Fig 6.11 MEDICI simulated electric field profiles at the interface for different stress conditions the drain voltage is fixed under $V_d$=7V.

However under $V_g$=$V_d$ stress condition two stage $N_{it}$ generation, with markedly different rates, separated by saturation region suggests two different interface state generation processes. The first process, which is very efficient in $N_{it}$ generation is dominant during early stage and saturates very quickly, while the second mechanism which has lower rate of $N_{it}$ generation leads to small degradation during long stress time. Degradation processes in which hot electron induced hydrogen release and creation acceptor type interface states play a crucial role is expected [23], [30]. In particular a greater role of hydrogen in early stage is expected when the rate of degradation is high.

In Fig. 6.12, the increase in $R_D$ vs. $\Delta I_{cp}$ (increase in interface states) taken from Figs. 6.9(a) and 6.9(b) is shown. The correlation between $\Delta R_D$ and $\Delta I_{cp}$ increase seen in Fig. 6.12 highlights the role of $N_{it}$ generation in the spacer damage. It is seen that nearly linear (slope: 0.8-0.85) relationship between $\Delta R_D$ and $\Delta I_{cp}$ under $I_{submax}$ and $V_g$~$V_t$ stress conditions clearly imply dominance of interface states generation in $R_D$ degradation during all the stages of degradation.

Under $V_g$=$V_d$ condition it can be observed from Figs. 6.9(a), 6.9(b) and 6.12 that initially $R_D$ degrades by $N_{it}$ generation. But between 1ms-10ms in the early stage there is more $R_D$ degradation than $N_{it}$ generation (slope greater than one in Fig. 6.12). This additional $R_D$

degradation can be attributed to trapping, which has been well known to occur under this stress condition. This implies that under $V_g=V_d$ condition, damage in the early stage occurs by a combination of $N_{it}$ generation and electron trapping. In the second stage after $R_D$ saturation upto 10 seconds it is seen that the small but finite increase in $R_D$ is due to $N_{it}$ generation. It is emphasised that these conclusions are valid only for technologies studied in this work.

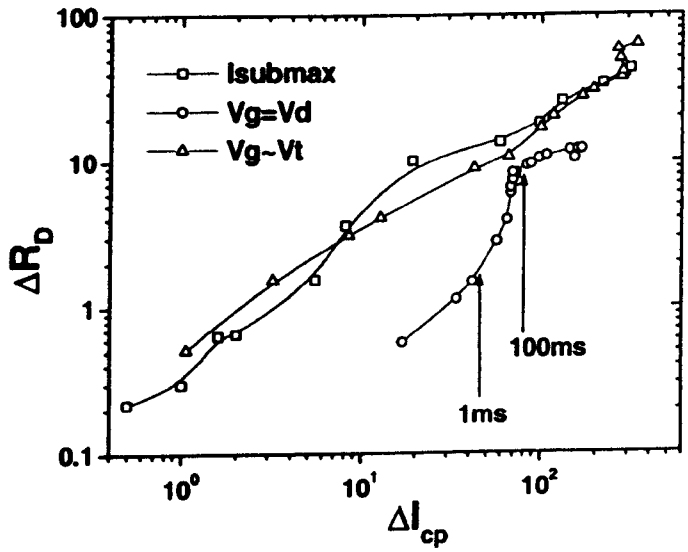


Fig. 6.12 The $R_D$ degradation vs. $I_{cp}$ ($N_{it}$) increase for the devices stress in Fig. 6.9, the time scale for which trapping is dominant under Vg=Vd stress condition is also highlighted

Thus, it is noted that under different stress conditions the majority of the damage in the spacer oxide occurs in the form of interface state creation. These results agree with the study of hot carrier degradation on CVD oxides in [30], [31]. The authors have confirmed that such oxides are more susceptible to the damage by interface state creation than by electron trapping. The degradation by higher generation of interface state in CVD oxides than by trapping could be accounted for by more hydrogenation during CVD process leading to larger density of hydrogen passivated Si dangling bonds at the interface in the spacer oxide.

### 6.5.3 Hole Trapping and Interface State Generation Under $V_g$~$V_t$ Stress Condition

While the hole trapping is known to occur under $V_g$~$V_t$ stress conditions, however for the devices under study it is observed that $g_m$ degradation (decrease) even under $V_g$~$V_t$, although the magnitude of $g_m$ degradation under $V_g$~$V_t$ condition is lower than that under $I_{submax}$

conditions under long term stress (Fig. 6.1). This points to the dominant role of interface states creation over hole trapping under $V_g$~$V_t$ for the technologies under investigation. This role of interface state generation over hole trapping is further investigated by constant base charge pumping measurements described in Sec. 6.5.2. In Fig. 6.13 the constant base charge pumping characteristics are shown for unstressed devices, devices stressed are under $V_g$~$V_t$ and $I_{submax}$ conditions at $V_d$=7.25V for 6000 seconds stress. This is followed by electron injection under $V_g$=$V_d$=7.5V condition, for 2 and 10 seconds for the device stressed under $V_g$~$V_t$, and for 10 seconds for the device stressed under $I_{submax}$ condition.

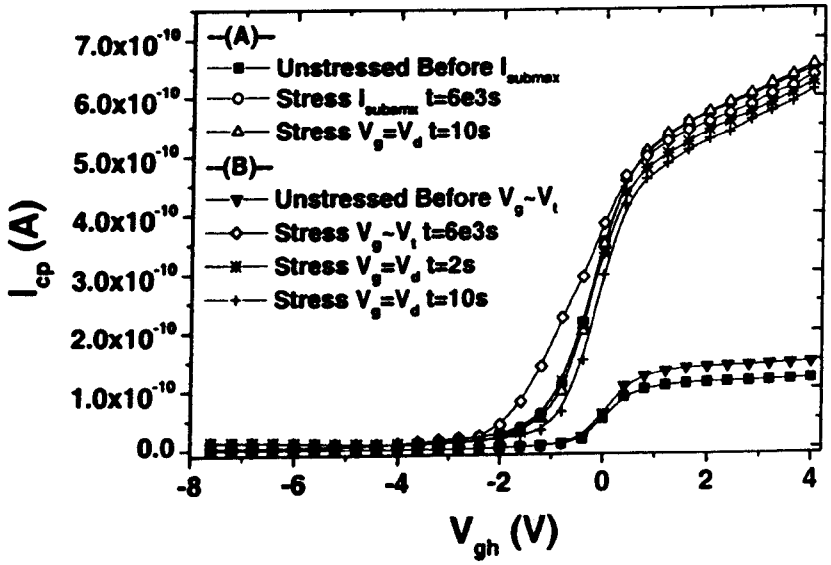


Fig. 6.13 Constant base charge pumping ($I_{cp}$) characteristics of: (A) unstressed device before stress under $I_{submax}$ condition (square), device stressed under $I_{submax}$ condition at $V_d$=7.25V for 6000 seconds (circle), electron injection (after stress under $I_{submax}$ condition) for 10 seconds under $V_g$=$V_d$=7.5V (up triangle), (B) unstressed device before stress under $V_g$~$V_t$ condition (down triangle), device stressed under $V_g$~$V_t$ condition at $V_d$=7.25V for 6000 seconds (diamond), electron injection (after stress under $V_g$~$V_t$ condition) for 2 seconds (star) and 10 seconds (plus) under $V_g$=$V_d$=7.5V.

It is noted that under both the conditions the $I_{cp}$ characteristics shift to the left due to the effect of interface charge and/or trapped positive charge [27]. However, it is seen from Fig. 6.13 that although the change in $I_{cp}$ current in saturation is marginally higher under $I_{submax}$ condition than under $V_g$~$V_t$ stress, the left shift of $I_{cp}$ characteristics is significantly more for stress under $V_g$~$V_t$. This is a characteristic shift due the presence of trapped positive charge [27].

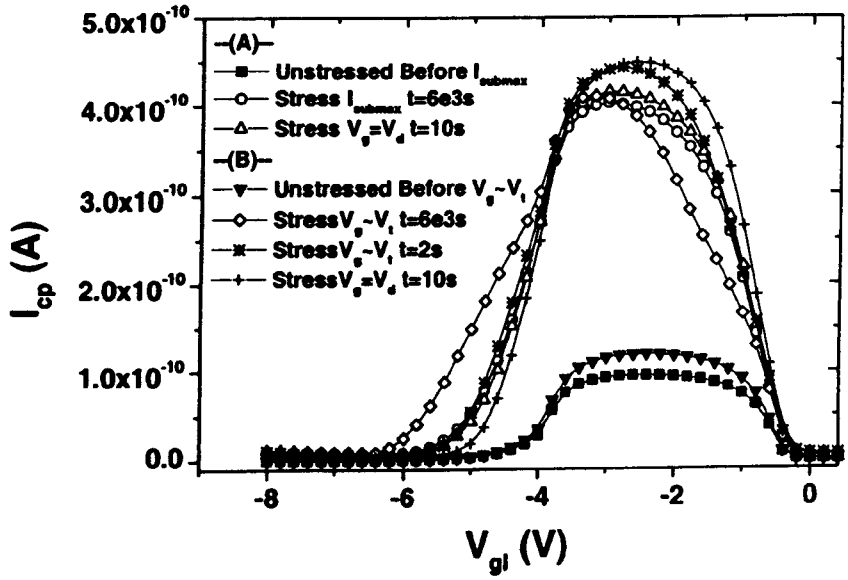


Fig. 6.14 Constant amplitude charge pumping characteristics for same set of experiments as in Fig. 6.13. The gate pulse frequency is 100kHz, and the magnitude of the charge pumping amplitude is 4V.

It should be mentioned that normally if there is a large positive trapped charge near the drain junction, a shoulder in $I_{cp}$ characteristics is seen (as discussed in Sec. 4.5.2.4, Fig. 4.9). But this shoulder is made less prominent in Fig. 6.13 due to dominance of interface states in these technologies for stress under $V_g$~$V_t$ condition. The shoulder in $I_{cp}$ characteristics is more apparent for the case of constant amplitude charge pumping [27] characteristics shown in Fig. 6.14 for the same set of measurements as in Fig. 6.13. This is due to the fact that in Figs. 6.13 and 6.14 for the same $V_{gh}$ level the $I_{cp}$ value for constant amplitude case is lower due to lesser charge pumping area probed than for the constant base charge pumping case.

The hole trapping under $V_g$~$V_t$ condition is further evidenced by right shifting of the charge pumping curve in Fig. 6.13 after brief electron injection phase for 2 seconds under $V_g$=$V_d$ stress condition due to neutralisation of trapped positive charge by injected electrons. A similar behaviour is also noted in Fig. 6.14. On the other hand, a similar electron injection phase after stress under $I_{submax}$ condition shown in Figs. 6.13 and 6.14 does not show any significant shift in the charge pumping characteristics even after 10 seconds.

The estimates of relative magnitude of trapped positive charge and interface states created under $V_g$~$V_t$ stress condition can be determined from the shift in charge pumping curve after

neutralisation of trapped holes using electron injection under $V_g=V_d$ stress, and increase in charge pumping current in saturation using (4.10), (4.9) [25], [26]:

$$Q_{ot} = \frac{\Delta V_{gh} C_{ox}}{q} \tag{6.17a}$$

$$N_{it} = \frac{\Delta I_{cp,max}}{qWf\Delta L_d} \tag{6.17b}$$

where $Q_{ot}$ is the trapped charge per unit area, $\Delta V_{gh}$ is the shift in the charge pumping curve after electron injection under $V_g=V_d$ stress condition for a given $I_{cp}$ value, $C_{ox}$ is the oxide capacitance per unit area, $N_{it}$ is the increase in interface states per unit area, $\Delta I_{cp,max}$ is the increase in saturation charge pumping current after stress, W is the device width, f is the gate pulse frequency, $\Delta L_d$ is the hot carrier damage length and q the electron charge.

In order to determine positive trapped charge after stress under $V_g \sim V_t$ condition, the value of $\Delta V_{gh}$ in equation (6.17a) has to be determined when hole neutralisation upon electron injection has occurred. This can be determined by noting from Fig. 6.13 that the $I_{cp}$ values in saturation under $I_{submax}$ and $V_g \sim V_t$ stress conditions are nearly equal, so the left shift of $I_{cp}$ curves after stress due to interface states alone should be approximately the same for both the stress conditions, since there are no positive charge created under $I_{submax}$ condition. Therefore, as seen in Fig. 6.13 the electron injection for 2 seconds after $V_g \sim V_t$ stress shifts the $I_{cp}$ curve to the right and merges (for $V_{gl}<0$) with that under $I_{submax}$ condition.

This indicates that at this point positive charge neutralisation is complete. The electron injection for a longer time period than 2 seconds after stress under $V_g \sim V_t$ condition further shifts the $I_{cp}$ curve to right as a result of filling of neutral electron traps that are created during stress under $V_g \sim V_t$ stress condition [24]. Therefore, from Fig. 6.13, for stress under $V_g \sim V_t$ condition for 6000 seconds and using maximum $V_{gh}$ shift value of about 0.5V, after electron injection for 2 second, the maximum positive trapped charge, $Q_{ot}$, value of $8.739 \times 10^{11} cm^{-2}$ is obtained. Whereas, using the value of $\Delta L_d$ approximately equal to the gate drain overlap (~500Å) length and the increase in charge pumping current in saturation an average interface state, $N_{it}$, value of $3.662 \times 10^{12} cm^{-2}$ is obtained. Further, from Fig. 6.13 for stress under $I_{submax}$ condition for 6000 seconds using increase in charge pumping current in saturation a $N_{it}$ value of $4.827 \times 10^{12} cm^{-2}$ is obtained.

From the values of $Q_{ot}$ and $N_{it}$ obtained under $V_g \sim V_t$ stress condition it is seen that the average value of interface states created is approximately four times the maximum value of the trapped positive charge. This could account for a reduction in $g_m$ seen after stress under $V_g \sim V_t$ condition. This effect will further be enhanced since it is possible that not all of the hole trapping is occurring at the drain channel junction and interface states are also created alongside the trapped charge [16] which reduces the effect of trapped charge. Therefore, the channel shortening effect of hole trapping [17], [18] on the linear drain current or $g_m$ is reduced and degradation (instead of increase) in $g_m$ or the linear drain current is observed as a result of increased carrier scattering due to the effect of trapped interface charge.

From the results of the calculated $N_{it}$ values from $I_{cp}$ measurements, it is noted that the interface state generation under $V_g \sim V_t$ stress conditions is lower than under $I_{submax}$ stress condition. This is also confirmed by results in Figs. 6.1 and 6.2, where a lower $g_m$ degradation for stress under $V_g \sim V_t$ stress than under $I_{submax}$ condition is noted. In Fig. 6.15 the result of $g_m$ degradation for the same sequence of stress experiments as in Figs. 6.13 and 6.14 are shown. It is noted that the sudden rise in $g_m$ degradation for electron injection after stress under $V_g \sim V_t$ condition is a result of trapped positive charge neutralisation and filling of neutral electron traps. On the other hand, there is no significant change in $g_m$ degradation for electron injection after stress under $I_{submax}$ condition consistent with results of $I_{cp}$ measurement shown in Figs. 6.13 and 6.14.

## 6.6 Saturating Series Resistance and Spacer Oxide Degradation

In the previous section it is argued that the early stage hot carrier damage is dominated by interface state generation under $V_g \sim V_t$ and $I_{submax}$ stress conditions, while it occurs by a combination of the interface state generation and trapping under $V_g = V_d$ condition. However, the causes of long term saturation in the series resistance degradation behaviour remain unclear. In this section long term spacer oxide degradation behaviour under different stress biases is examined. It has been reported that hot carrier degradation of LDD n-MOSFETs shows a saturating behaviour after long stress time [32]-[36], [29]. This saturating behaviour has been attributed, variously, to the increase in barrier height to injection as a result of already injected carriers [32], shift in location of the peak electric field due to localised trapped charge [33], saturating nature of degradation length [36] or saturation [29] of available defect precursors, like hydrogen passivated Si bonds and other defect sites that exist near the Si-$SiO_2$ interface.

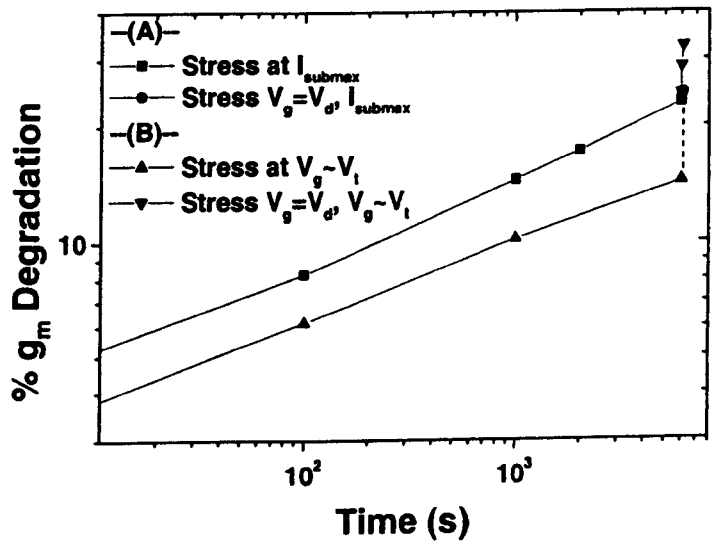


Fig. 6.15 Results of $g_m$ degradation for the sequence of stress experiments shown in Figs. 6.13 and 6.14.

In Fig. 6.16 the results of $R_D$ degradation behaviour at different drain biases under different stress conditions are shown. It is seen that the magnitude of $R_D$ degradation in the early stage depends on the stress bias thus, the larger the stress bias, the more the damage in the early stage. The $R_D$ degradation behaviour under $V_g$~$V_t$ and $I_{submax}$ conditions is very similar in the second stage. This is also evident from $I_{cp,max}$ increase seen in Fig. 6.9(a) for these stress conditions. This implies that $R_D$ degradation due to the damage in the spacer oxide continues to occur by interface state creation. Chung et. al. [37] have also confirmed this conclusion, where they have shown that, under $I_{submax}$ condition, the damage in the spacer oxide is dominated by interface state generation. It is also noted from Fig. 6.16 that the $R_D$ saturation under $V_g$~$V_t$ and $I_{submax}$ tends to reach the same level after long stress time, although the saturation level under $V_g$~$V_t$ stress condition is slightly higher than that for the corresponding $I_{submax}$ condition. Further, under both these conditions, the $R_D$ degradation shows a gradually saturating behaviour instead of a threshold level for saturation.

The saturation mechanisms proposed in [32], [33] cannot account for the observed saturating behaviour in these devices. Firstly, the barrier height to injection is not significantly affected during stress under $V_g$~$V_t$ and $I_{submax}$ conditions, since most of the created acceptor type interface states will not be charged during stress under these conditions. This is because the Fermi level close to the drain is separated from the conduction band for $V_g \leq V_d/2$ stress

conditions. So, the alteration of barrier height to injection [32] or shift in the position of peak electric field [33] as a probable cause of saturation of $R_D$ degradation under $V_g \sim V_t$ and $I_{submax}$ can be discounted.

The saturation by inversion of $n^-$ LDD region [35] also cannot account for the observed $R_D$ degradation behaviour, as such a mechanism would imply a threshold level for saturation, after which no degradation will be observed when the $n^-$ LDD region is inverted. The slowly saturating $R_D$ behavior under $V_g \sim V_t$ and $I_{submax}$ conditions suggests a degradation mechanism in which the rate of degradation depends on the number of defect precursors available for the damage in the spacer region as proposed in [29]. There are a finite number of defect precursors available for the damage in the spacer region: as the density of the available precursors is depleted with the damage, the rate of interface state creation is reduced which eventually leads to a saturation in $R_D$ degradation.

The increased barrier height to injection under $V_g=V_d$ stress condition, due to negative charge in the oxide, is one of the contributing factors to the saturation, observed until about 10 seconds of $R_D$ degradation under this condition. Since the majority of the created interface states under this condition will be charged in addition to the negatively trapped charge this negative charge will repel further injection of electrons, leading to a saturation effect.

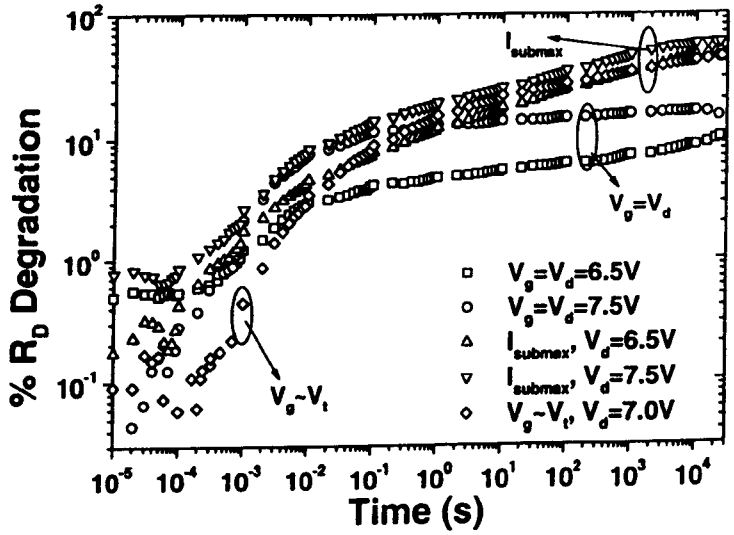


Fig. 6.16 Evolution of the drain series resistance ($R_D$) degradation for the three stress conditions under different drain biases.

It is seen from Fig. 6.16 that under long term stress there is a small but finite increase in $R_D$ degradation after about 100 seconds under $V_g=V_d$ conditions. The same effect is also observed in Fig. 6.9(a) where a small increase in $I_{cp,max}$ in long term stress is seen, as pointed out in Sec. 6.5.2. This increase in $R_D$ degradation after saturation under $V_g=V_d$ stress condition could be correlated with an increase in $I_{cp,max}$ seen in Fig. 6.9(a), implying that in the long term degradation the damage occurs by a lower rate of interface state generation as seen in Fig. 6.9 (a).

From the study of $R_D$ degradation behaviour it is found that the hot carrier degradation of the spacer oxide shows different characteristics than that of grown oxide. In particular, lesser role of trapping under $V_g \sim V_t$ and $I_{submax}$ conditions is observed as seen from $R_D$ degradation curves and increase in charge pumping current measurements, although this mechanism is well known to occur for the gate oxides [17], [18]. The power law degradation observed for the gate oxides have exponents usually between, 0.3-0.5 under all bias conditions, but $R_D$ degradation by the damage in the spacer oxide shows a saturating two stage degradation with slopes of 0.4-0.5 in the early stage and 0.15-0.18 in the long term degradation. Based on the discussion above, the mechanisms of hot carrier degradation of LDD n-MOSFETs under study can be summarised as follows:

1. Hot carrier degradation in the spacer oxide proceeds in two stages. In the early stage, the degradation begins by interface state creation for all the three stress conditions. The amount of degradation in this stage depends on hot carrier injection fluence into the spacer oxide, more the injection flux larger the degradation. In the second stage, although the degradation still continues to occur by interface state creation, the rate is lower compared to that in the early stage.

2. During the second stage between 1-10 seconds, the damage starts to become significant in the gate oxide above the $n^-$ LDD and channel regions, which begins to degrade the accumulation layer and inversion layer mobility.

## 6.7 Summary

In this chapter the detailed degradation behaviour of 5V technologies is presented. A methodology is developed that de-couples the increase in the drain series resistance from the mobility. The results of the drain series resistance degradation demonstrate a two stage

saturating degradation in the spacer oxide, while the mobility degradation by the damage in the gate oxide dominates in the late stage. The nature of hot carrier degradation of the spacer oxide beginning from microseconds is investigated using alternate injection experiments and charge pumping measurements. It is seen that under $V_g \sim V_t$ and $I_{submax}$ stress conditions, the damage by interface state generation shows two stage saturating characteristics. Under $V_g = V_d$ stress conditions the contribution of both interface state generation and trapping is observed consistent with previous studies, while under $V_g \sim V_t$ and $I_{submax}$ stress conditions the damage is reported to be dominated by interface state generation. It is observed that the magnitude of the damage in the early stage depends on the stress bias, implying that the amount of the damage depends on the hot carrier injection fluence. The saturation of the drain series resistance under $V_g \sim V_t$ and $I_{submax}$ stress conditions is attributed to a finite number of defect sites available for the damage in the spacer oxide and depletion of these defect precursor with the hot carrier damage leads to saturating behaviour.

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# CHAPTER 7

# DEGRADATION OF 3V AND 2V TECHNOLOGIES-THE REDUCING EXTRACTED SERIES RESISTANCE

## 7.1 Introduction

The conventional LDD technologies optimised for 5V operation have been very successful in reducing the hot carrier degradation in submicron regimes. However, as the channel lengths are pushed into sub-half micron regime, device scaling requires, along with the other device dimensions, proportionately scaled operating voltage to meet power and reliability (hot carrier and gate oxide) requirements. This has led to a generation of new technologies, with 3V, 2V based operating voltage standards. Conceptually these technologies are similar to LDD technologies, apart from the fact that the LDD and channel doping for these technologies is much higher than for the 5V generation and they may have specially engineered drain doping profile, for example GOLD [1] or LATID [2] etc. However, they still retain conventional spacer isolation in their fabrication process flow, with the source/drain transition regions offsetting the $n^+$ region from the rest of the source/drain structure.

Because of this transition region and the existence of the spacer for isolation, these technologies are still very much susceptible to degradation associated with series resistance increase [2]. Although, due to higher drain doping in the transition region, this degradation is expected to be considerably lower than that for 5V technology reported in Chapter 6. On the other hand, due to reduced channel length and operating voltage the peak electric field in these technologies is expected to be higher, causing more damage in the channel region. Therefore, in the optimisation of these technologies, the relative roles of the channel and spacer damages need to be quantified and carefully monitored.

In this Chapter, following the series resistance and mobility degradation extraction methodology used in the analysis of hot carrier degradation of 5V technologies, the results of the degradation behaviour of 2V and 3V technologies are presented. It is seen that for these technologies the conventional series resistance and mobility extraction procedure results in

reducing extracted series resistance. This is demonstrated to be due to the dominance of the channel damage as a result of scaling. The analysis of the effect of scaling on peak electric field and the extent of the damage in the channel region show that in these technologies there is a significant deviation of universal mobility behaviour as seen in the broadening of the $g_m$ degradation after stress. This deviation in the universal mobility behaviour is the origin of factitious reducing extracted series resistance obtained with conventional extraction methodology of Chapter 6. This highlights the need for a new extraction methodology, incorporating the effect of damage in the channel region on universal mobility behaviour.

## 7.2 Series Resistance and Mobility Degradation

The series resistance and mobility degradation is extracted using the methodology based on (6.8):

$$R_{ON} = \frac{1}{\beta}\gamma\frac{1}{(V_{gs} - V_t - \alpha V_{ds})} + \frac{\theta}{\beta}\gamma + R_{SD} \qquad (7.1)$$

An extraction procedure similar to that outlined in Sec. 6.2 is followed. The value of the parameters $\theta$ and $R_{SD}$ are extracted for each technology using the L-array method and, are used in (7.1) to obtain the drain series resistance and the mobility ($\beta$) degradation.

### 7.2.1 Series resistance and mobility degradation of 3V technology

The typical degradation behaviours of $R_D$, mobility ($\beta$) along with measured transconductance for comparison are shown in Figs. 7.1, 7.2 and 7.3, for $V_g \sim V_t$, $I_{submax}$ and $V_g = V_d$ stress conditions respectively. In contrast to the results obtained for 5V technologies, it is noted from Figs. 7.1-7.3, a reducing extracted series resistance (negative percentage degradation) for all the stress conditions. It is seen that initially, depending upon the stress condition there is a small but finite increase in $R_D$. But as the mobility degradation becomes dominant, the extracted series resistance starts to decrease. Further, the comparison of $g_m$ and mobility degradation, shows that for all the stress conditions mobility degradation follows $g_m$ degradation very closely, implying that in these technologies mobility degradation, and hence damage in the channel region, plays a dominant role in determining the device degradation.

For $I_{submax}$ condition, where hot carrier damage is maximum, a long-term saturating behaviour in $g_m$ and mobility degradation is seen, which could be attributed to the finite number of

defect precursors available for damage. Further, as discussed above, due to higher doping in the LDD region in these technologies (c. f. Table 4.1), a lesser series resistance degradation is expected. However, the reduction in the extracted series resistance is not clear at this stage and is a matter of discussion in Sec. 7.3 below.

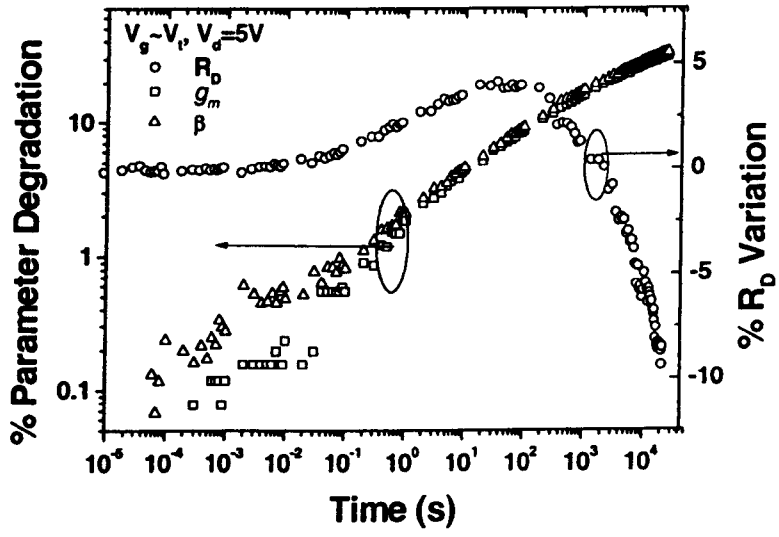


Fig. 7.1 Extracted drain series resistance ($R_D$), mobility (β) along with maximum experimental $g_m$ degradations for 0.36μm, 3V technology device stressed under $V_g$~$V_t$, $V_d$=5V condition.

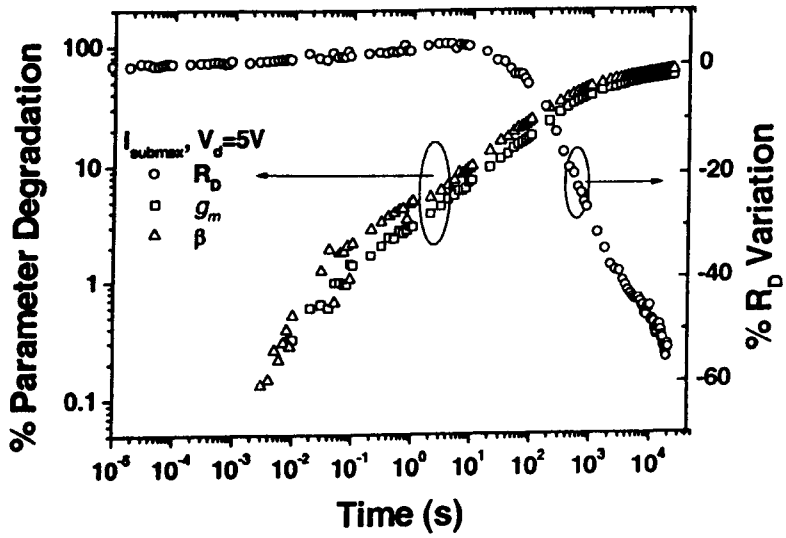


Fig. 7.2 Extracted drain series resistance ($R_D$), mobility (β) along with maximum experimental $g_m$ degradations for 0.36μm, 3V technology device stressed under $I_{submax}$, $V_d$=5V condition.

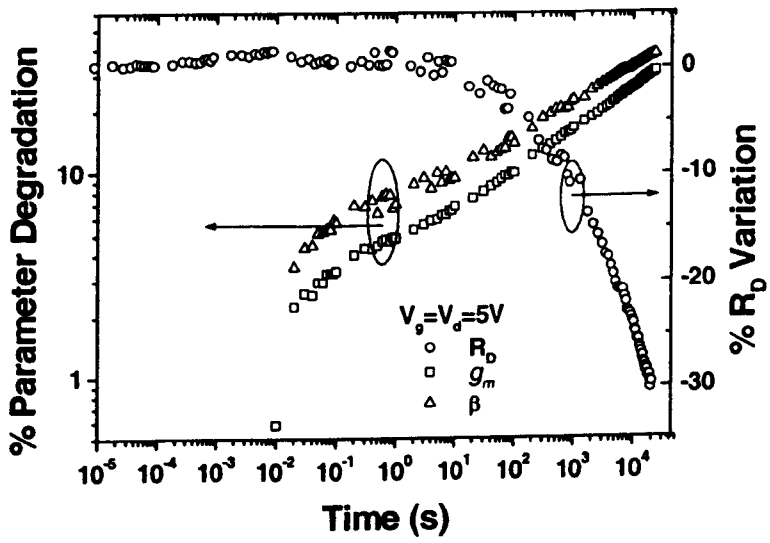


Fig. 7.3 Extracted drain series resistance ($R_D$), mobility (β) degradation along with maximum experimental $g_m$ degradation for 0.36μm, 3V technology device stressed under $V_g=V_d=5V$ condition.

## 7.2.2 Series Resistance and Mobility Degradation of 2V Technologies

The typical extracted series resistance, mobility and maximum experimental $g_m$ degradation behaviours using (7.1) for 2V technologies under $V_g \sim V_t$, $I_{submax}$ and $V_g=V_d$ stress conditions are shown in Figs. 7.4, 7.5 and 7.6 respectively. It can be noted that, similarly to 3V technologies, a reduction in extracted $R_D$ is obtained. In this case, however, the worst case $R_D$ reduction is much greater than that for the 3V case. It is noted that in general the amount of degradation depends on the stress condition and is maximum for $I_{submax}$ stress and is lowest for $V_g=V_d$ stress condition. Further, it is noted that, like 3V-degradation case, mobility degradation follows experimental $g_m$ degradation and a long term saturation in both $g_m$ and extracted mobility degradation is also observed.

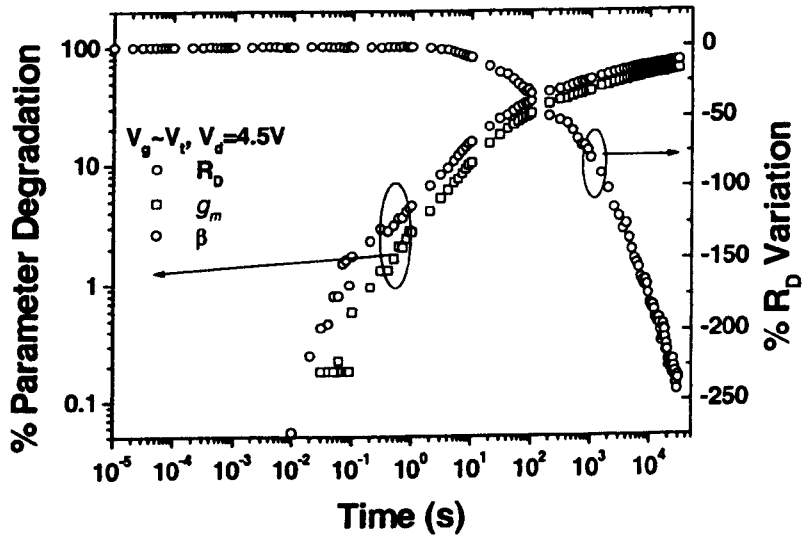


Fig. 7.4 Results of extracted drain series resistance ($R_D$), mobility (β) along with maximum experimental $g_m$ degradation for 0.32μm, 2V technology device stressed under $V_g$~$V_t$, $V_d$=4.5V condition.

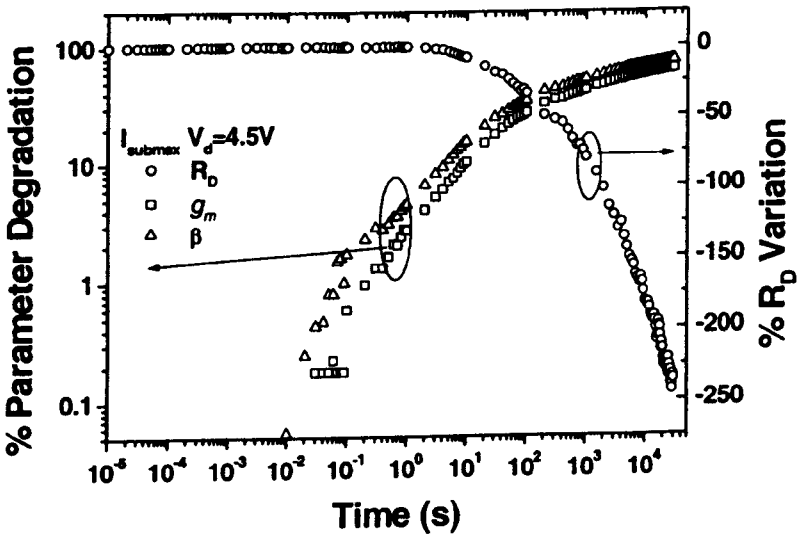


Fig. 7.5 Results of extracted drain series resistance ($R_D$), mobility (β) along with maximum experimental $g_m$ degradation for 0.32μm, 2V technology device stressed under $I_{submax}$, $V_d$=4.5V condition.

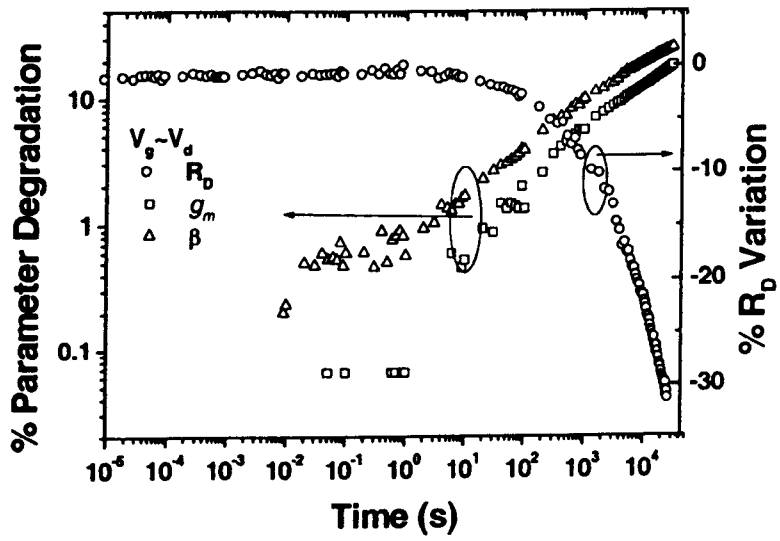


Fig. 7.6 Results of extracted drain series resistance ($R_D$), mobility (β) along with experimental $g_m$ degradation for 0.32μm, 2V technology device stressed under $I_{submax}$, $V_g$=$V_d$=4.5V condition.

### 7.2.3 A Discussion on Reducing Series Resistance

One of the key difference in the degradation behaviour of 5V technologies and that of 2V and 3V technologies, also noted in Chapter 5, is that $V_t$ degradation observed for 2V and 3V technologies is much higher than that for 5V technologies. This is seen in Fig 7.7, in which experimental $V_t$ degradation for 5V, 3V and 2V devices under $I_{submax}$ stress condition are compared. It is noted that for a device under stress as the operating voltage and channel lengths are reduced, the corresponding $V_t$ degradation increases, implying greater damage in the channel region with scaling.

This increase in $V_t$ can also be correlated to the stress time when extracted $R_D$ degradation starts to reduce for 3V and 2V devices, as seen in Fig. 7.8. In Fig. 7.8 the normalised change in $R_D$ is shown for the devices in Fig. 7.7. It is seen from Figs. 7.7 and 7.8 that for 5V technologies, where the $V_t$ change is very small, the drain series resistance increases. On the other hand, for 3V and 2V technologies, as $V_t$ degradation increases a decrease in series resistance is observed, marked by arrows in Fig. 7.7 and 7.8. Further, it is noted that the larger the $V_t$ degradation, the higher is the reduction in the extracted series resistance. This clearly connects the damage to the channel region as cause of decrease in extracted series resistance.

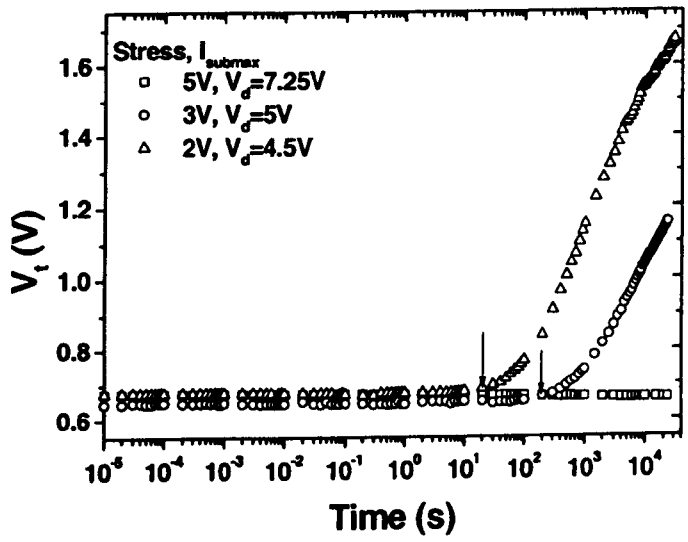


Fig. 7.7 Comparison of threshold voltage degradation behaviour of 5V, 3V and 2V technologies under $I_{submax}$ stress condition.

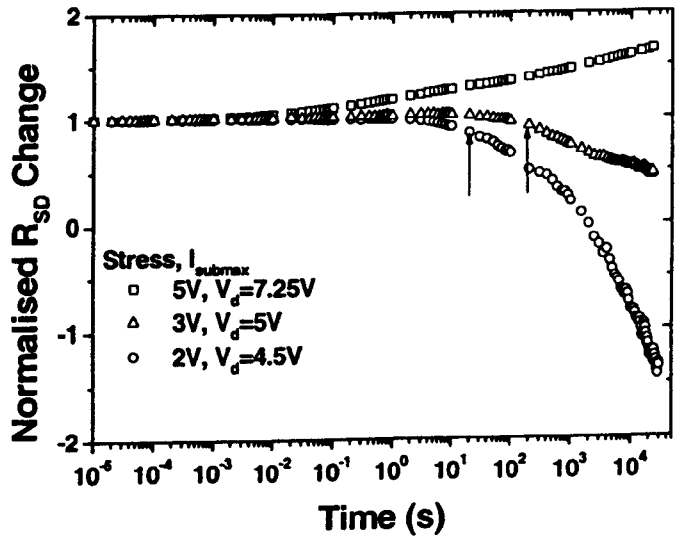


Fig. 7.8 Normalised change in extracted series resistance ($R_{SD}$) for 5V, 3V and 2V technologies under $I_{submax}$ stress condition.

The large $V_t$ degradation observed for 2V and 3V technologies can be attributed to the large damage in the channel region. It is well known that hot carrier damage is localised near drain-channel junction and the length of the damaged region (~0.1μm) does not scale significantly with channel length [3]. This is also confirmed by the simulated lateral electric field profiles

using the 2D-device simulator MEDICI [4] for 5V and 2V technologies, as shown in Figs. 7.9 and 7.10 respectively. In the simulations for each technology, $V_d$ is fixed at typical experimental stress voltage with the gate voltages emulating different stress conditions from $V_g \sim V_t$ through $I_{submax}$ to $V_g=V_d$. It is noted that with scaling, the peak electric field under stress increases and its location shifts towards channel. However, the lateral extent of the high field region (taken here as ~$1x10^5$V/cm or higher corresponding to large impact ionisation) is nearly constant in both cases.

The effect of this localised damage on magnitude of degradation in device parameters like $V_t$ or $g_m$ depends on the channel length [3], [5]. It has been shown that the screening effect due to the built-in potential and the drain bias, influences the effect of the localised negative interface charge on device parameters like $V_t$ [6]. This screening effect depends in general on channel length, value of the interface charge and extent of the damage.

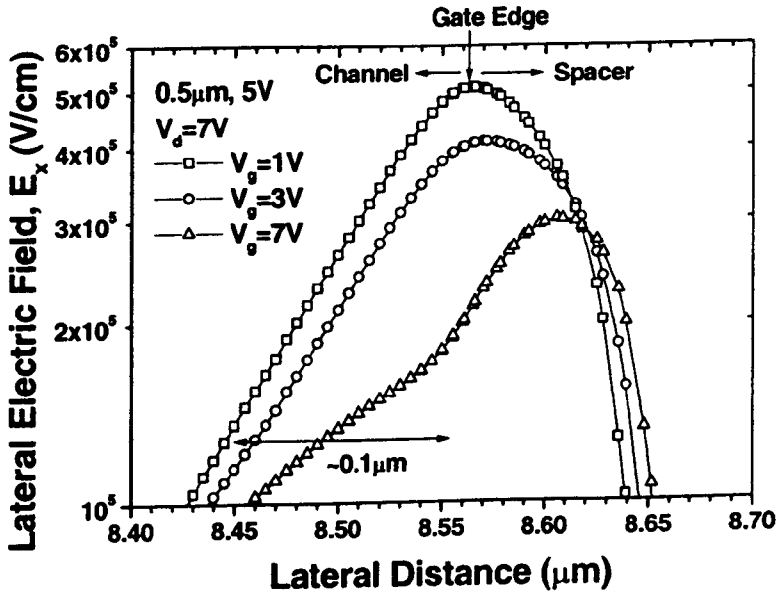


Fig. 7.9 MEDICI simulated lateral electric field profiles for different gate voltages at fixed drain bias $V_d$=4.5V for 0.5μm, 5V technology at $V_d$=7V.

In order to study the effect of extension ($\delta L_d$) of the localised damage in the drain region following the approach used in [6], the experimental device structures in the linear region of operation were simulated and the effect of $\delta L_d$ on threshold voltage was studied. In the simulations, the threshold voltage is defined as the minimum gate voltage required to obtain surface potential of $2\phi_B$. A fixed interface charge of different extensions from the gate-drain

edge is placed in the channel region. In Fig. 7.11 the change in $V_t$ normalised to its maximum value as a function $\delta L_d$ is shown for 0.32μm, 2V and 0.5μm, 5V technologies.

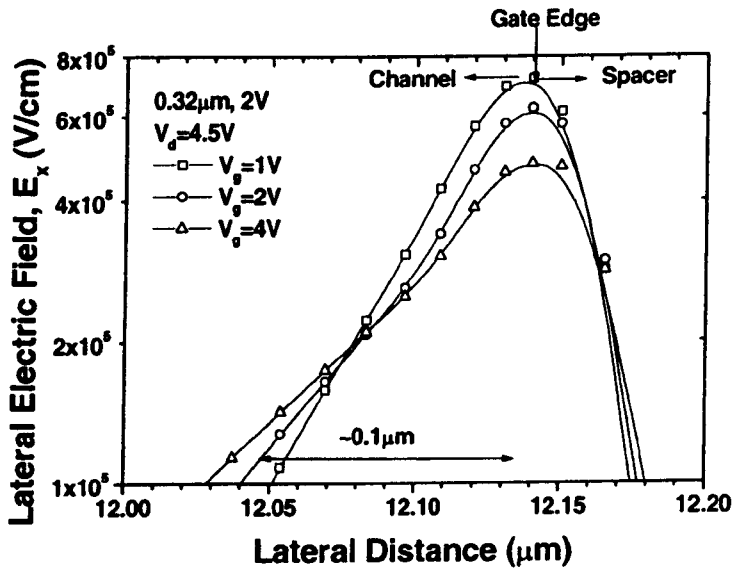


Fig. 7.10 MEDICI simulated lateral electric field profiles for different gate voltages at fixed drain bias $V_d$=4.5V for 0.32μm, 2V technology.

It is noted that for fixed $\Delta N_{it}$ the increase in the $V_t$ depends on $\delta L_d$. For small values of $\delta L_d$ (<0.05μm), the $V_t$ degradation is insignificant but as $\delta L_d$ increases $V_t$ also increases. The value of $\delta L_d$ for which maximum change in $V_t$ ($\sim q\Delta N_{it}/C_{ox}$) is obtained increases with channel length and for the same value of $\delta L_d$ the change in $V_t$ is lower for the longer channel length. For typical hot carrier damage length of about 0.1μm (Figs. 7.9 and 7.10) the change in $V_t$ for 0.32μm device is nearly 90% of the maximum value, whereas it is only 50% for a 0.5μm device.

Thus, it is seen that for channel length of 0.32μm the value of $\delta L_d$ of about 0.1μm leads to maximum change in $V_t$. The same is true for channel lengths below 0.32μm and, in general, for devices with length approaching quarter micron (or less) regime. This explains the large

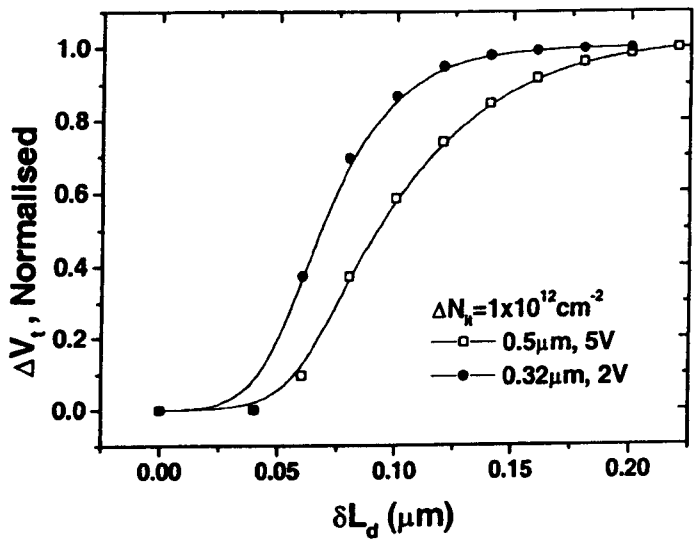


Fig. 7.11 Normalised change in threshold voltage as a function of extension $\delta L_d$ of interface charge ($N_{it}$) placed from the gate-drain edge for 0.32μm, 2V and 0.5μm, 5V technologies.

$V_t$ degradation, as seen for 2V and 3V technologies. The larger proportion of the degraded channel at these short channel lengths also affects the behaviour of other device parameters like $g_m$ and mobility. Since for these devices the length of the damage free region is reduced, the carriers traverse through damaged region for longer distances. This implies that carriers will suffer more scattering due to charge in the damage region, and as a result, their effect on $g_m$ and mobility behaviour becomes more pronounced as compared to longer channel length devices.

In order to observe the effect of stress on effective mobility behaviour, the device mobility is extracted using

$$\mu_{eff} = \frac{Lg_d}{WQ_{inv}(V_g, V_d)} \tag{7.2}$$

where $g_d$ is the device conductance, $Q_{inv}$ is the inversion layer charge and is obtained as

$$Q_{inv} = C_{ox}(V_{gs} - V_{t0} - \delta V - V_{ds}/2) \tag{7.3}$$

where $V_{t0}$ is the threshold voltage of the stressed device, $C_{ox}$ is the oxide capacitance per unit area and $\delta V$ is the change in threshold voltage after stress.

In Fig. 7.12, the extracted mobility curves before and after stress are shown for 2V device under $I_{submax}$ stress condition. It is noted that the peak mobility decreases after stress while shifting to higher $V_g$ values and the rate of fall of mobility in universal region reduces. This indicates a change in mobility behaviour after stress.

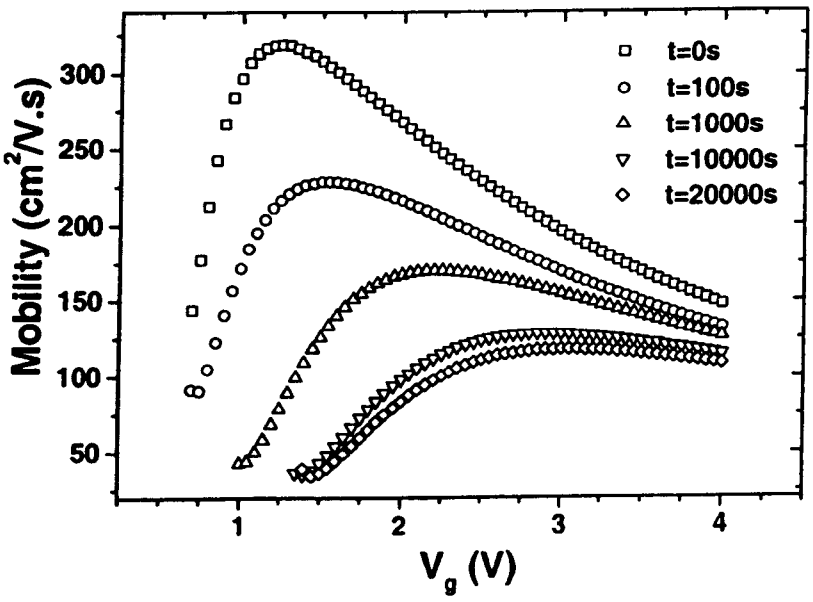


Fig. 7.12 Extracted effective mobility curves ($\mu_{eff}$-$V_{gs}$) before and after different stress time for 0.32μm, 2V device stressed under $I_{submax}$, Vd=4.5V condition.

The reduction in effective mobility seen in Fig. 7.12 can be attributed to Coulomb scattering of electrons in the inversion layer and/or increased drain series resistance. However the origin of change in mobility behaviour is not directly evident. At first sight it points to a reduction in $R_D$ after hot carrier stress. But the amount of reduction in $R_D$, as obtained for these technologies, cannot be explained on the basis of physical arguments only, since in extraction for severely degraded devices even zero or negative extracted $R_{SD}$ values are obtained. From physical arguments, on the contrary, $R_D$ is expected to increase for hot carrier stressed LDD n-MOSFETs. This is because hot carrier stress creates negative charge in oxide in the form of acceptor type interface states and/or trapped charge including that in spacer region [6]-[9]. The generation of negative charge in spacer region will always cause an increase in $R_D$ due to the depletion of the underlying $n^-$ layer.

As shown above, the large $V_t$ change observed for these devices after stress is due to a significant fraction of channel length damaged by hot carrier stress. The charge in the damaged channel region also affects the mobility behaviour and results in change in universal model parameters. As a consequence, the assumption in (7.1) that the universal model parameters remain constant after stress becomes invalid and results in reducing extracted series resistance observed in Figs. 7.1-7.6. The study of the effect of the interface charge on the universal mobility behaviour is the topic of the next Chapter.

## 7.3 Summary

In this Chapter it is demonstrated that conventional series resistance and mobility degradation extraction methodology developed in Chapter 6, is inadequate in describing channel and spacer degradation behaviour for device technologies with channel lengths approaching quarter micron regime. Although this model gives the mobility degradation behaviour, which is physically plausible, but it gives decreasing extracted series resistance, which can not be explained on the basis of physical arguments. It is seen that as device technologies are scaled, an increasing fraction of channel region is damaged by hot carrier stress, thus resulting in greater channel damage. The Coulomb scattering by interface charge in the damaged channel region causes changes in the mobility behaviour, which is not considered in the conventional extraction methodology, thus resulting in decreasing extracted series resistance.

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# CHAPTER 8

# MODELLING THE EFFECT OF OXIDE CHARGE ON UNIVERSAL MOBILITY BEHAVIOUR

## 8.1 Introduction

With the continuous reduction of oxide thickness in CMOS devices, the damage to the oxide layer due to charge injected by FN and Direct Tunnelling (DT) becomes a serious concern even under normal operating conditions [1]. In addition to inherent oxide reliability concern, this damage also affects device electrical performance due to change in parameters like transconductance, threshold voltage and mobility. The increase in the interface charge causes Coulomb scattering of inversion layer carriers and degrades carrier mobility. It has been well known that the inversion layer mobility follows a universal relationship independent of the substrate impurity [2], [3]. This relationship has been crucial in device modelling and circuit simulation tools like BISIM and SPICE. Although the effect of interface charge on device mobility has been well established, its effect on universal behaviour is not well analysed.

In this Chapter the effect of oxide damage due to interface state generation on n-MOS inversion layer mobility, is examined. It is seen that the conventional universal mobility model is unsatisfactory in describing behaviour in the presence of significant interface charge. The role of Coulomb scattering in determining the change in this behaviour is discussed. As a result of stress, the universal mobility model becomes interface charge dependent. It is seen that the effect of interface damage attributed to the Coulomb scattering in the region of strong inversion can be described by a change in universal model parameters with interface charge ($N_{it}$).

## 8.2 Experimental Setup

In order to determine the effect of interface charge on mobility behaviour it is needed to stress the device in which damage is generated in the channel region, while the spacer region is not damaged. To achieve this, the hot carrier generation under the spacer region needs to be eliminated while injecting carriers in the gate oxide causing damage in the channel region. Two techniques, which have been widely used to study the gate oxide degradation in the

channel region, are the substrate hot electron/hole (SHE/SHH) injection [4], [5] or the Fowler-Nordheim (FN) injection. In these techniques carriers are injected into the gate oxide by applying suitable gate bias. Since the spacer region is not under the direct gate control, using these techniques carrier injection into the spacer region can be avoided and consequently the damage in the spacer region can be eliminated. However, SHE injection requires special injector structures in comparison to FN injection, which can be readily implemented in normal MOS devices. Therefore, FN stress is used in this work to achieve uniform oxide degradation.

The devices both from 2V and 3V technologies are used. An HP4140B Pico-ammeter unit is used to implement stress and low level current measurements, including linear $I_{ds}$-$V_{gs}$ and charge pumping measurements. In the experiments used in this study, constant voltage FN stress is employed as shown in the schematic representation of Fig. 8.1(a) with the gate voltages varying between 5.5V-7V. Under this arrangement the electrons tunnel from channel into the gate and gain energy from the applied gate voltage as shown in Fig. 8.2(b). On reaching the gate some of the energetic electrons release secondary species believed to be hydrogen or hot holes at the polySi-$SiO_2$ interface which can move back into the oxide towards Si-$SiO_2$ interface [6], [7]. The movement of these species through oxide creates defects in the bulk oxide and interface states at Si-$SiO_2$ interface. Therefore, by using FN stress, the effect of oxide charge in the channel region on mobility behaviour can be determined.

The damage after FN stress is characterised by measurement of linear $I_{ds}$-$V_{gs}$ characteristics at $V_{ds}$=0.05V, 0.1V. The inversion layer effective mobility ($\mu_{eff}$) is determined from linear $I_{ds}$-$V_{gs}$ characteristics

$$\mu_{eff} = \frac{Lg_d}{WQ_{inv}(V_g, V_d)} \tag{8.1}$$

where $g_d$ is the channel conductance, L is the drawn gate length, W is the device width, $Q_{inv}$ is the inversion layer charge.

The inversion layer charge can be approximated by the gate overdrive [8]

$$Q_{inv} = C_{ox}\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right) \tag{8.2}$$

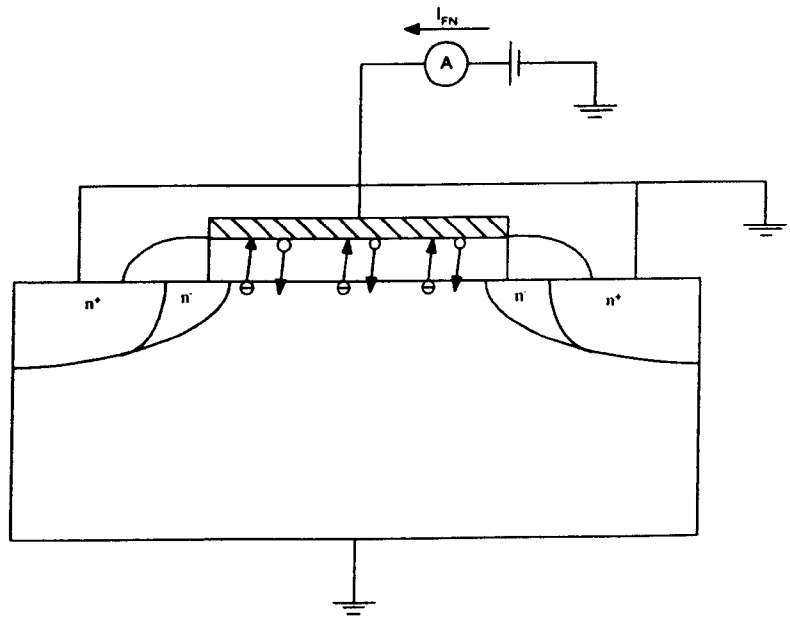


Fig. 8.1(a) Schematic experimental FN stress setup.

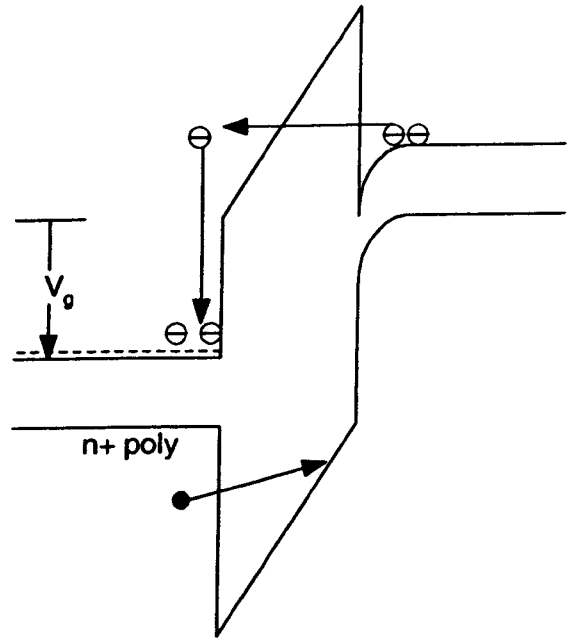


Fig. 8.1(b) Energy band diagram under FN stress, the secondary carrier generated by tunnelling electron on reaching $n^+$ poly-Si gate electrode is believed to be hydrogen and/or hole.

The interface charge generated by FN stress is determined from constant base charge pumping ($I_{cp}$) characteristics [9]. In these measurements a series of gate pulses of frequency 100kHz is applied to the gate, with the base of the gate pulse ($V_{gl}$) held constant at –4V while high level of the gate pulse ($V_{gh}$) is swept from low value close to $V_{gl}$ to high value above device threshold voltage. The increase in interface states ($\Delta N_{it}$) generated after stress is determined from the increase in saturation charge pumping current ($\Delta I_{cp}$) using the equation below [9]:

$$\Delta N_{it} = \frac{\Delta I_{cp}}{qfWL} \tag{8.3}$$

where q is the electronic charge, f is the gate pulse frequency. In (8.3) it is assumed that interface states are generated uniformly over the channel region under FN stress. The effective mobility has been shown to follow the well-known universal behaviour given by [2]

$$\mu_{eff} = \frac{\mu}{1+(E_{eff}/E_c)^{\gamma}} \tag{8.4}$$

where $E_c$ and $\gamma$ are empirical constants and $E_{eff}$ is effective normal field experienced by inversion layer electrons and is determined from [8] as

$$E_{eff} = \frac{1}{\varepsilon_{Si}}\left(Q_d + \frac{Q_{inv}}{2}\right) \tag{8.5}$$

where $Q_d \sim (4\varepsilon_{Si}N_A\phi_B/q)^{1/2}$ is the depletion layer charge at the onset of inversion. Using (8.2) and (8.3) the effect of interface charge generated by FN stress on universal mobility behaviour (8.4) is studied.

## 8.3 Deviation of Universal Mobility Behaviour

Typical effective electron inversion layer mobility curves obtained from (8.1) for different values of interface charge for 2V technology stressed at $V_{gs}$=5V are shown in Fig. 8.2. After stress, there is a reduction in peak effective mobility due to increased Coulomb scattering by generated interface charge ($\Delta N_{it}$) as well as a reduction of slope of effective mobility curve in the low field region (below peak). It is further noted that, with stress, the position of the peak

effective mobility shifts to higher $E_{eff}$ values and the degradation of effective mobility in the universal region reduces with the effective field.

This leads to a reduced rate of fall of universal mobility with stress and causes deviation of universal mobility behaviour from unstressed device [3]. Solid lines in Fig. 8.2, which are obtained by fitting universal model (8.6) to the corresponding mobility curves in Fig. 8.2 with the parameter $\mu$ degradation due to Coulomb scattering by interface charge [10] according to (8.6), illustrates this deviation.

$$\mu_{eff} = \frac{\mu_0 /(1+\alpha\Delta N_{it})}{1+(E_{eff}/E_c)^{\gamma}} \tag{8.6}$$

It is observed that the conventional model does not accurately describe the change in universal model behaviour after stress, highlighting the need for a modified universal model to account for this deviation.

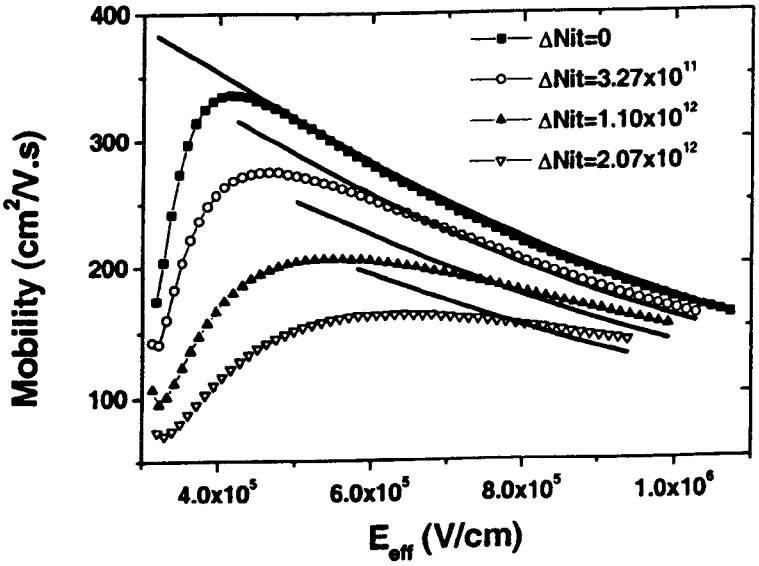


Fig. 8.2 Variation of effective mobility obtained from (8.1) for different values of interface states ($\Delta N_{it}$ in $cm^{-2}$). The lines show fit by universal curve where only $\mu$ is varied in (8.6) with $E_c$ and $\gamma$ fixed to unstressed values.

It has been shown in [11] from theoretical considerations, that screened Coulomb scattering of inversion layer carriers can account for the deviation of universal behaviour with interface charge. The effective electron inversion layer mobility is determined by Coulomb mobility

($\mu_c$), phonon mobility ($\mu_{ph}$), and surface roughness mobility ($\mu_{sr}$), which can be combined using Matthiessen rule [12]

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_c} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} \tag{8.7}$$

Fig. 8.3 shows a schematic diagram of $E_{eff}$ dependence of the various components of $\mu_{eff}$ and resulting $\mu_{eff}$-$E_{eff}$ curves with increasing interface charge at room temperature. In Fig. 8.3, $\mu_{c1}$ refers to Coulomb mobility of unstressed device while $\mu_{c2}$ and $\mu_{c3}$ are Coulomb mobilities with increasing values of interface charge. For unstressed device at low $E_{eff}$ (low inversion layer density) $\mu_{eff}$ is limited by Coulomb scattering due to the depletion layer charge ($\mu_{c1}$ in Fig. 8.3) and $\mu_{eff} \sim \mu_c$. As $E_{eff}$ is increased, the increased inversion layer charge screens the depletion layer charge and Coulomb mobility increases. A maximum in $\mu_{eff}$ is observed when screening is nearly complete and $\mu_{c1}$ becomes very large. At this $E_{eff}$ value $\mu_{eff}$ starts to be dominated by combination of phonon and surface roughness scattering, which leads to the observed universal behaviour.

However when interface charge increases due to degradation caused by stress, an additional Coulomb scattering with interface charge reduces the mobility in the low field region [3], [11]. For low interface charge of $1\text{-}5\text{x}10^{10}\text{cm}^{-2}$, the inversion layer is able to screen the interface charge and the mobility behaviour remains unchanged. But when the interface charge increases and becomes a significant fraction ($\sim 10^{11}\text{cm}^{-2}$, few tenths or more) of the inversion layer density the screening effect is only partial even in the high field region and depends both on inversion layer density and interface charge.

This results in a reduced Coulomb mobility in high field region. Therefore, there is a significant effect of Coulomb mobility with increasing $N_{it}$ shown as $\mu_{c2}$ and $\mu_{c3}$ in Fig. 8.3 on overall mobility behaviour in the universal regime (after peak). In general the deviation is proportional to the interface charge. It should be mentioned that the screening effect also affects the phonon and surface roughness scattering but their affect should be less significant as compared to screened Coulomb scattering [11], [13].

## 8.4 Modified Universal Model

As a result of FN stress both charge in the oxide and at Si-$SiO_2$ interface are generated. But to study the mobility degradation the effect of interface charge primarily needs to be considered. It is reported in [11] that the magnitude of carrier scattering in the channel by oxide charge depends on its location from the Si-$SiO_2$ interface. For the charge at the interface (as in interface states) the scattering is maximum, while it rapidly decreases as the location of the trapped charge moves away from the interface.

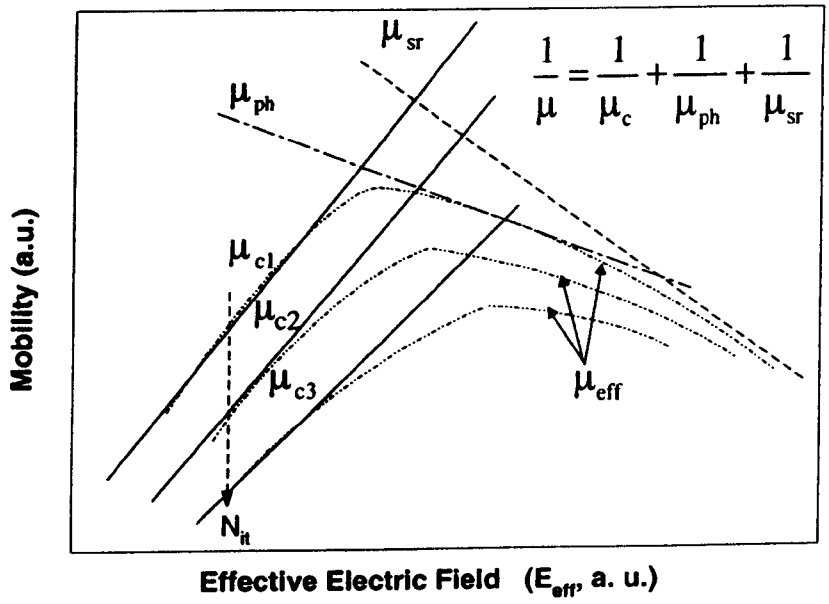


Fig. 8.3 Schematic diagram showing various components of effective mobility.

It has been shown in [14] using charge centroid measurement that after FN stress the trapped charge is located near the middle of the oxide. Thus very little trapped charge exits in the immediate vicinity of the interface resulting in the reduced carrier scattering due to the trapped charge. The scattering of the carriers by the trapped oxide charge is further reduced in the presence of interface charge due to shielding of oxide charge by the interface charge. So for charge trapped in the bulk oxide their effect on channel mobility should be negligible. Therefore, the effect of trapped charge on device behaviour is mainly to increase the threshold voltage whereas the interface states will affect both mobility and threshold voltage.

Although the approach used in [11] predicts the deviation of mobility behaviour in the universal region, it does not give a closed form analytic model which can be incorporated in device models to predict their performance after stress. The effect of interface charge on

universal behaviour is shown in Fig 8.4.which shows the effective mobility behaviour normalised to its maximum values before and after FN stress.

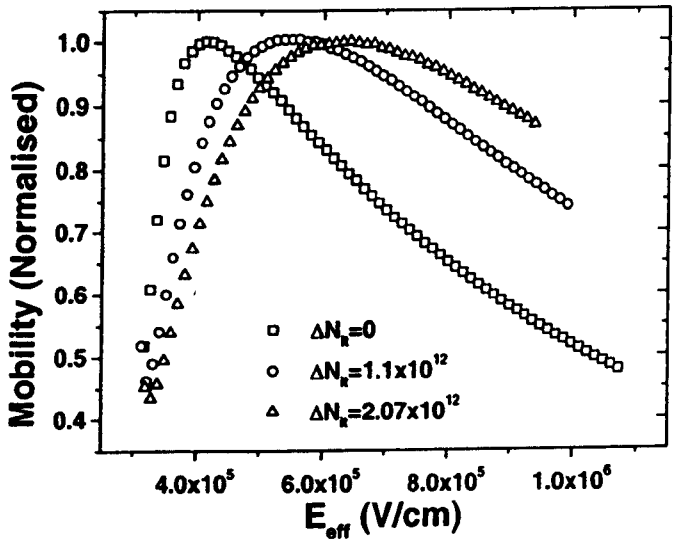


Fig. 8.4 Normalised experimental effective mobility vs. effective field ($\mu_{eff}$-$E_{eff}$) curves for unstressed and after different values of interface charge ($\Delta N_{it}$ in $cm^{-2}$) generated after FN stress for 0.32μm, 2V device. The FN stress gate voltage is 6.5V.

It is noted that as a result of the generated interface charge after stress, the maximum of the mobility curve shifts to higher $E_{eff}$ values and there is reduced rate of fall of mobility in the universal region. This deviation can be accounted for by allowing parameter $E_c$ to change with $N_{it}$. The effect of the oxide charge on effective mobility was studied by Sun and Plummer using an effective mobility model of the form [10]

$$\mu_{eff} = \mu_{max}\left(\frac{E_c}{E_{eff}}\right)^{Cl} \tag{8.8}$$

where $\mu_{max}$, $E_c$ and Cl are constants. In this model, the effect of oxide charge on mobility behaviour is described by following dependence of parameters $\mu_{max}$ and $E_c$ on interface charge

$$\mu_{max} = \frac{\mu_0}{1+\alpha\Delta N_{it}} \tag{8.9}$$

$$E_c = E_{C0}Ae^{B\Delta Nit} \tag{8.10}$$

where $\mu_0$, $\alpha$, $E_{c0}$, A and B are parameters. However this model does not accurately represent the universal behaviour of the modern device technologies as seen in Fig. 8.5 for a 2V technology device. It is seen that (8.8) gives very poor match to effective mobility behaviour. Thus the effect of interface charge on universal model parameters needs to be evaluated considering universal model (8.4).

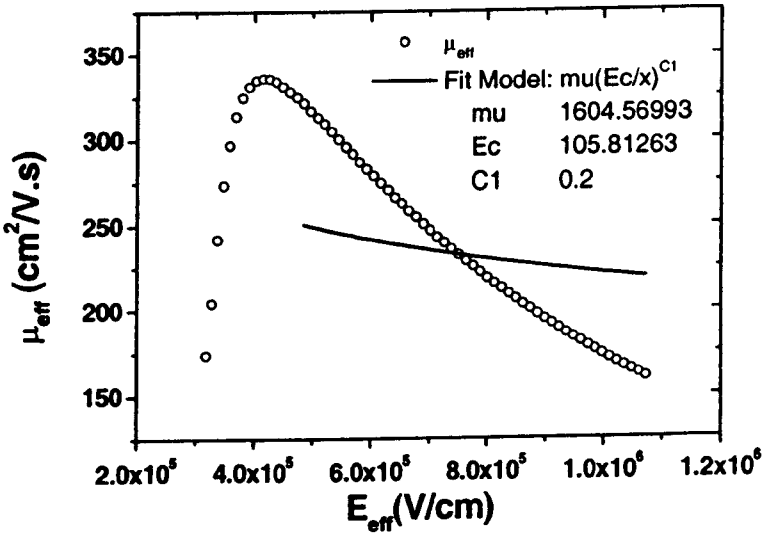


Fig. 8.5 Typical fit to experimental effective mobility using the model in [10].

The effective field dependence of the universal mobility model (8.4), taking into account series source-drain resistance, can be expressed as

$$\mu_{eff} = \frac{\mu}{1 + (E_{eff}/E_c)^{\gamma} + 2R_{SD}\mu\varepsilon_{Si}(W/L)(E_{eff} - E_d)} \tag{8.11}$$

For FN stressed device (8.11) is fitted to $\mu_{eff}$ in the universal region in Fig. 8.2. The value of $R_{SD}$ in (8.11) is fixed to its unstressed value and the parameters $\mu$, $E_c$ and $\gamma$ are extracted after every FN stress period and their behaviour as a function of interface charge is analysed. Fig. 8.6 shows the variation of mobility $\mu$ as function of generated interface charge ($N_{it}$). It is seen that the mobility degradation with $N_{it}$ due to coulomb scattering can be described by relation [10]

$$\mu = \frac{\mu_0}{1 + \alpha\Delta N_{it}} \tag{8.12}$$

with value of parameter $\alpha$~$5.5x10^{-13}cm^{-3}$ for the devices used in this study.

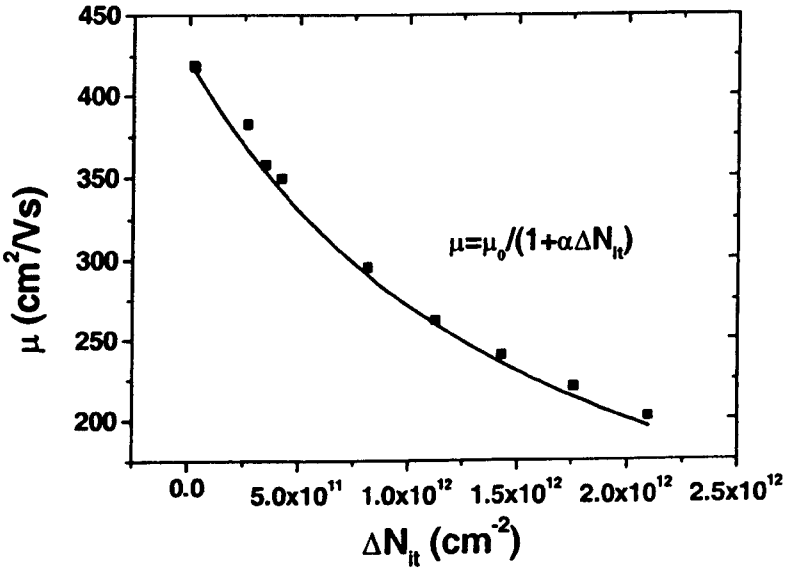


Fig. 8.6 Results of universal mobility parameter $\mu$ variation as function interface charge ($\Delta N_{it}$) obtained from (8.3) for FN stressed device

In Figs. 8.7, the variation with $N_{it}$ is shown for parameter $E_c$. It is seen that the parameter $E_c$ increases exponentially with $N_{it}$ and can be modelled by the relation

$$Ec = E_{c0}e^{B\Delta Nit} \qquad (8.13)$$

where $E_{c0}$ is the $E_c$ value for unstressed device and B is parameter with values given in Table. 8.1.

Table 8.1

| $\mu=\mu_0/(1+\alpha\Delta N_{it})$ | $E_c=E_{c0}e^{B\Delta N_{it}}$ |
|---|---|
| $\mu_0=418cm^2/V.s$ | $E_{c0}=1.16x10^6V/cm$ |
| $\alpha=5.5x10^{-13}cm^{-3}$ | $B=3.5x10^{-13}cm^{-2}$ |

Although relations (8.12) and (8.13) are empirical in nature they signify the effect of Coulomb scattering on universal mobility behaviour. Crucially, these relations enable to

obtain a closed form analytic model for the stressed device and, for the purpose of device modelling, they adequately describe the effect of the interface charge on the universal mobility behaviour.

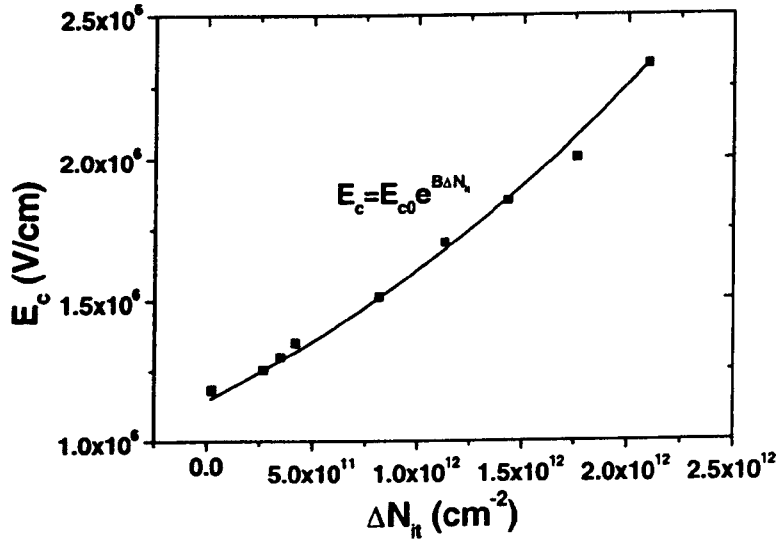


Fig. 8.7 Variation of universal model parameters $E_c$ with the interface charge ($\Delta N_{it}$) extracted from (8.3) for FN stressed device in Fig. 8.6.

Based on (8.12) and (8.13), the modified universal mobility model can be expressed as

$$\mu_{eff} = \frac{\mu_0}{(1+\alpha\Delta N_{it})\left(1+\left(\frac{E_{eff}}{E_{c0}e^{C\Delta Nit}}\right)^{Y_0}\right)+2R_{SD}\mu_0\varepsilon_{Si}(W/L)(E_{eff}-E_d)} \qquad (8.14)$$

The variation of model parameters $\mu$ and $E_c$ in (8.14) forms the basis of the new extraction methodology presented in Chapter 9, where the effect of the localised channel damage after hot carrier stress on the universal mobility model is described by the modified form (8.14).

## 8.5 Summary

In this Chapter the effect of the interface charge generated using FN stress on the universal mobility behaviour is studied. It is seen that the degradation in the form of the interface charge leads to a deviation in the universal mobility behaviour. In the approach presented in this Chapter, the deviation is modelled as change in the universal model parameter $E_c$ in addition to mobility parameter $\mu$. Using this approach, a modified universal model is

developed, which accurately reflects device behaviour after stress. This study also highlights the importance of incorporating the modified universal model in simulation tools like BSIM and SPICE for deep sub-micron technologies, where effects of hot carrier and gate current stress are a concern even under normal operating conditions. Furthermore, as discussed in the next Chapter, the modified universal model is crucial for hot carrier stress, as the damage in the channel region is expected to cause similar deviation.

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# CHAPTER 9

# A NEW METHODOLOGY FOR PARAMETER EXTRACTION AFTER HOT CARRIER STRESS

## 9.1 Introduction

The hot carrier degradation is a serious concern in deep submicron MOS technologies. In order to meet stringent lifetime criteria, as channel length is reduced, specially engineered drain structures are implemented to reduce the lateral electric field [1]-[3]. This is achieved with the help of a combination of ion implantation and spacer isolation technologies and devices with graded junction profiles such as LDD [4], LATID [5] have now become an integral part of modern CMOS technologies. Although these technologies have been successful in reducing hot carrier effects, it is recognised that they can suffer from enhanced degradation associated with spacers [6], [7]. It has been reported that along with channel mobility degradation, these technologies suffer from degradation associated with higher series resistance [7]-[10]. Reduced drain doping results in a large series resistance and its increased susceptibility to the damage in the spacer region, whereas increased drain doping increases the peak electric field and can cause large damage in the channel region leading to mobility degradation. Therefore, in an effort to optimise the performance of these devices, a trade-off between electrical performance and reliability has to be achieved.

Since both series resistance and mobility play a vital role in determining overall device degradation behaviour and lifetime prediction [7]-[10], it is important to delineate and quantify their relative roles. In the early studies, series resistance and mobility degradation were analysed qualitatively by comparing linear drain current degradation at high and low gate voltages respectively [7], [8]. In a method based on conventional series resistance and effective channel length extraction known as L-array method [11], the series resistance degradation is obtained by stressing devices of different channel lengths from the same technology [9]. This method requires that drain voltage during stress be continuously regulated, such that equal distribution of damage for different channel lengths is obtained. It predicts series resistance degradation to a good accuracy provided the damage in all the devices can be accurately controlled. A single device based method has been reported in [12]

but require substantial amount of measurement data and associated numerical computational costs can be high.

In another class of modified L-array methods, the mobility is modelled by first order universal relation [13], [10] for devices with different channel lengths and conventional L-array method is then applied to find universal model parameter, mobility and series resistance for unstressed device. The series resistance and mobility degradation of the stressed device is then determined from linear on resistance, knowing values of unstressed device parameters. This simple and easy to implement method extracts series resistance and mobility degradations with minimum measurements and provides a good insight into behaviour of channel and spacer damages [10].

All the methods outlined above make an implicit assumption that the I-V model of a stressed device can be described by that of the unstressed device with damage in the channel region modelled by degradation in mobility parameter $\mu$ and threshold voltage. This assumption amounts to considering the damage in the channel after hot carrier stress as uniform, which is not true. Further, all these studies assume that there is no change in the universal mobility model as result of the charge generated by the stress, which is also not true as seen in Chapter 7. While these methods hold good for long channel length devices or for the cases where the damage in the channel region is small, they have limited application when studying the degradation behaviour of device technologies in deep submicron regime. It is seen in Chapter 7 that for device technologies in quarter-micron regime, where the fraction of the channel region damaged by hot carrier stress becomes significant, the conventional extraction procedure results in reducing extracted series resistance, highlighting the deficiencies associated with this approach [14]. In order to evaluate hot carrier degradation performance of technologies in deep submicron regime, a method is therefore required which can quantify the roles of degradation associated with spacer and channel regions and overcome inadequacies of the current methodologies.

In this Chapter a new single device based methodology for extraction of series resistance and mobility components of the degradation is presented. This methodology addresses the decreasing series resistance problem encountered with conventional extraction methodology reported in Chapter 7. In this methodology the hot carrier stressed device is modelled by separately considering on resistance of the undamaged channel and that of degraded channel.

It uses the universal mobility model [15] for a better accuracy in the modelling of channel resistance, unlike the first order model used in conventional methods [10], [13], [14]. A modified universal model, taking into account the effect of interface charge developed in Chapter 8 using FN stress experiments, is incorporated into model equations of the on resistance damaged channel. It is then successfully applied to the extraction of series resistance and mobility degradations for a range of 2V, 3V and 5V technologies, showing its generality. The stability of the method is demonstrated by considering the effect variation of model parameters on extracted device parameters. Further, the method is validated by comparing the experimental and calculated device parameters like transconductance $g_m$, threshold voltage $V_t$ and 2D device simulations, correlating extracted series resistance with those obtained from simulations.

## 9.2 The New Methodology

### 9.2.1 Linear Resistance of Unstressed Device

The linear on resistance ($R_{ON}$) of an LDD MOSFET given by the sum of channel resistance ($R_{CH}$) and series source-drain series resistance ($R_{SD}$) can be expressed as

$$R_{ON} = R_{CH}(V_{gs}) + R_{SD}(V_{gs}) \tag{9.1}$$

where $R_{SD}(V_{gs})$ is composed of bias dependent intrinsic resistance (determined by accumulation layer and spreading resistances) and resistance of the rest of the series source and drain ($R_{SD}=R_S+R_D$) ohmic regions. Following the approach reported by [16] the intrinsic source-drain resistance ($R_{INT}$) can expressed as

$$R_{INT} = \frac{1}{\mu_{eff} C_{ox} W/\Delta L} \frac{1}{(V_{gs} - V_t - V_{ds}/2)} \tag{9.2}$$

where $\mu_{eff}$ is the effective electron mobility, $C_{ox}$ is the oxide capacitance, W is the device width, $\Delta L$ is the average length of the source-drain overlap regions, $V_t$ is the threshold voltage and other symbols have their usual meanings. Using (9.2) and the well-known expression for channel resistance, $R_{ON}$ becomes

$$R_{ON} = \frac{1}{\mu_{eff} C_{ox} W/L} \frac{1}{(V_{gs} - V_t - V_{ds}/2)} + R_{SD} \tag{9.3}$$

where $L \cong L_{eff} + \Delta L$, with $L_{eff}$ as effective channel length.

In strong inversion region the effective mobility ($\mu_{eff}$) can be modelled by universal mobility model given by Eq. 2.32 [15]

$$\mu_{eff} = \frac{\mu}{1 + (E_{eff}/E_{c0})^{\gamma_0}} \tag{9.4}$$

where $E_c$, $\gamma$ are empirical constants representing the effect of the vertical field on channel mobility. Eq. (9.4) can be expressed in terms on the terminal voltages as (Eq. 2.33)

$$\mu_{eff} = \frac{\mu_0}{1 + \theta_0 (V_{gs} + V_t - V_{ds}/2)^{\gamma_0}} \tag{9.5}$$

where $\theta_0 = (1/6 t_{ox} E_{c0})^{\gamma 0}$. With effective mobility model given by (9.5), (9.3) can be expressed as

$$R_{ON} = \frac{1}{\mu_0 C_{ox} W/L} \frac{1 + \theta_0 (V_{gs} + V_t - V_{ds}/2)^{\gamma 0}}{(V_{gs} - V_t - V_{ds}/2)} + R_{SD} \tag{9.6}$$

### 9.2.2 Linear Resistance Model for Stressed device

After hot carrier stress, the device is damaged both in the channel as well as spacer regions, degrading threshold voltage, channel mobility and series resistance. The distribution of the damage is well known to be non-uniform and localised near drain region, following the electric field profile in general. The precise resistance of this region can be obtained if exact distribution of the damage after stress is known, which cannot be determined from the present measurements. In this approach to an approximation this non-uniform damage is replaced by an equivalent uniformly damaged region with an average interface charge density $\Delta N_{it}$. The charge density $\Delta N_{it}$ here is interpreted as net charge density at the interface as result of interface states and any oxide charge influencing carrier mobility. Using these assumptions the stressed device of channel length L can then be modelled as undamaged device of channel length $L_0$ and uniformly damaged device of length $\delta L$, with $L = L_0 + \delta L$. This is illustrated in Fig. 9.1, along with the resistance contribution of the various regions of a stressed device. Although the extent of the damage region can increase after stress, it has been reported that its value does not change significantly as function of the stress [17]-[19]. Therefore, in this

approach it is assumed that the value of the extent of the damage afters stress remains fixed to a quantity δL.

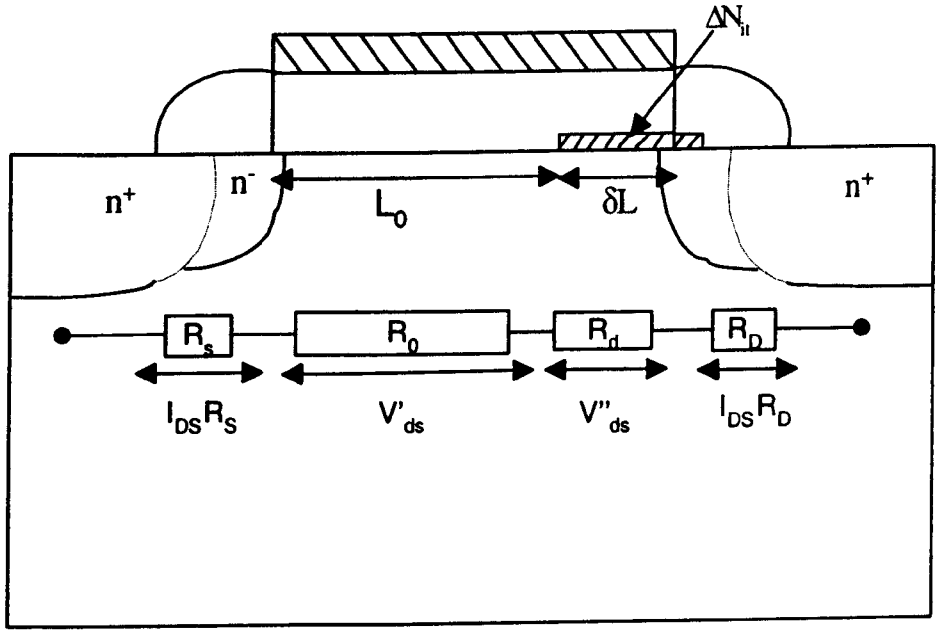


Fig. 9.1 Schematic representation of a hot carrier damaged device consisting of undamaged channel region of length $L_0$ and damaged region of extent δL with uniform interface charge $\Delta N_{it}$.

As shown in Fig. 9.1, the linear on resistance of the stressed device can be expressed as sum of resistances of undamaged, $R_0(V_{gs})$ and damaged $R_d(V_{gs})$ regions, plus the series source drain resistance $R_{SD}$

$$R_{ON} = R_0(V'_{gs}) + R_d(V'_{gs}) + R_{SD} \tag{9.7}$$

The resistance $R_0(V'_{gs})$ of the undamaged channel with the universal mobility model can be obtained from (9.6) as

$$R_O(V'_{gs}) = \frac{1}{\mu_0 C_{ox} W/L_0} \frac{1+\theta_0(V'_{gs}+V_{t0}-V'_{ds}/2)^{\gamma_0}}{(V'_{gs}-V_{t0}-V'_{ds}/2)} \tag{9.8}$$

where V'gs and V'ds are the gate and drain voltages across undamaged channel and $\theta_0=(1/6t_{ox}E_{c0})^{\gamma 0}$ and $\gamma_0$ are universal model parameters of the unstressed device.

For evaluating the resistance of the damaged channel, the deviation in the universal mobility model discussed in Chapter 8 needs to be taken into account. In the calculation of the

effective field, given by 2.28, for stressed device, term $Q_d$ in (2.28) remains fixed after stress, since it is actually determined by the depletion layer charge at the onset of inversion, which remains fixed, determined by the substrate doping. The interface charge of the stressed device only affects the term $Q_i$ in (2.28) and can be expressed as

$$Q_i = C_{ox}(V_{gs} - V_{t0} - \delta V - V_{ds}/2) \tag{9.9}$$

where $\delta V$ is the change in the threshold voltage of the damaged region after stress. Taking into account the variation of parameters $\mu$ (8.9) and $E_c$ (8.10) in the damage region the modified universal mobility model can be expressed as

$$\mu_{eff} = \frac{\mu/(1+\alpha\Delta N_{it})}{1+\theta(V_{gs}+V_{t0}-\delta V-V_{ds}/2)^{\gamma}} \tag{9.10}$$

where, $\theta=(1/6t_{ox}E_{c0})e^{-B\gamma 0\Delta Nit} = \theta_0 e^{-C\Delta Nit}$, while $V''_{gs}$ and $V''_{ds}$ are the gate and drain voltages across damaged region. The values of other parameters in (9.10) i. e. $\alpha$ and B are obtained from Table 8.1.

Using the modified universal mobility model (9.10), the linear resistance of damaged devices can be expressed as

$$R_d = \frac{(1+\alpha\Delta N_{it})}{\mu_0 C_{ox} W/\delta L}\,\frac{1+\theta_0 e^{-C\Delta Nit}(V'_{gs}+V_{t0}-sq\Delta N_{it}/C_{ox}-V'_{ds}/2)^{\gamma_0}}{(V'_{gs}-V_{t0}-sq\Delta N_{it}/C_{ox}-V'_{ds}/2)} \tag{9.11}$$

The parameter s in the threshold voltage increase ($\delta V=sq\Delta N_{it}/C_{ox}$) of damaged channel represents the effect of the drain 2D field on surface potential and threshold voltage of the damaged device. As discussed in Sec. 7.2.3, the 2D screening effect of build-in potential and applied drain bias in the drain channel junction, lowers the threshold voltage increase due to localised damage near drain region. As shown in [20] the amount of increase in the threshold voltage for given amount damage depends on the extension of the damage and the actual amount of the charge. This screening effect on threshold voltage is represented here by parameter s ($\leq 1$) and for a given amount of charge $q\Delta N_{it}$ the threshold voltage increase is approximated by $sq\Delta N_{it}/C_{ox}$. It should be noted that in general parameter s is expected to vary with stress time due to increase in charge in the damaged region. However an approximate value of s for a given extension $\delta L$ can be determined from simulated increase in threshold

voltage of the damaged region as function of channel length and localised charge as shown in Fig 7.11 (further discussed in Sec. 9.2.3).

The quantities $V'_{gs}$, $V''_{gs}$ and $V'_{ds}$ and $V''_{ds}$ are calculated as follows:

The total applied drain voltage as shown in Fig. 9.1 is the sum of the voltage drops across source and drain series resistances, undamaged channel and damaged regions. This can be expressed as

$$V_{ds}=I_{ds}(R_D+R_S) + V'_{ds}+V''_{ds} \tag{9.12}$$

The drain voltage across the channel is given by

$$V_{ch} = V'_{ds}+V''_{ds} =V_{ds}-I_{ds}(R_S+R_D) \tag{9.13}$$

In the linear region of operation, channel voltage can be approximated to vary linearly from source to drain, so $V'_{ds}$ and $V''_{ds}$ can be approximated as

$$V'_{ds}=(V_{ch}/L)L_0 \tag{9.14}$$

$$V''_{ds}=(V_{ch}/L)\delta L \tag{9.15}$$

The gate to source voltages across the damage and undamaged regions are given by

$$V'_{gs}=V_{gs} - I_{ds}R_S \tag{9.16}$$

$$V''_{gs}=V_{gs} - (I_{ds}R_S+V'_{ds}) \tag{9.17}$$

Using (9.12), (9.16) and (9.17) the term $(V'_{gs}-V'_{ds}/2)$ in (9.8) and $(V''_{gs}-V''_{ds}/2)$ in (9.11) can be expressed as

$$(V'_{gs}-V'_{ds}/2) = V_{gs} - I_{ds}R_S -1/2(V_{ds}-I_{ds}(R_D+R_S)-V''_{ds}) \tag{9.18}$$

$$(V''_{gs}-V''_{ds}/2) = V_{gs} - (I_{ds}R_S+V'_{ds}) - 1/2(V_{ds}-I_{ds}(R_D+R_S)-V'_{ds}) \tag{9.19}$$

With approximation $I_{ds}R_S \sim I_{ds}R_D$, (9.18) becomes $V_{gs}-1/2(V_{ds}-V''_{ds})$, and (9.19) reduces to $V_{gs}- 1/2(V_{ds}+V'_{ds})$. Using these approximations in (9.8) and (9.11) the total on resistance $R_{ON}$ of the hot carrier stressed device can by written as

$$R_{ON} = \frac{1}{\mu_0 C_{ox} W/L_0} \frac{1+\theta_0[V_{gs}+V_{t0}-\frac{1}{2}(V_{ds}-V^{*}_{ds})]^{\gamma_0}}{[V_{gs}-V_{t0}-\frac{1}{2}(V_{ds}-V^{*}_{ds})]} + \frac{(1+\alpha\Delta N_{it})}{\mu_0 C_{ox} W/\delta L} \frac{1+\theta_0 e^{-C\Delta Nit}[V_{gs}+V_{t0}-\frac{sq\Delta N_{it}}{C_{ox}}-\frac{1}{2}(V_{ds}+V^{'}_{ds})]^{\gamma_0}}{[V_{gs}-V_{t0}-\frac{sq\Delta N_{it}}{C_{ox}}-\frac{1}{2}(V_{ds}+V^{'}_{ds})]} + R_{SD} \quad (9.20)$$

In order to apply (9.20) to a hot carrier stressed device and study degradation of mobility and series resistance separately, the parameters $\theta_0$, $\gamma_0$ and $R_{SD}$ for unstressed device need to be found. The value of $R_{SD}$ for unstressed device can be determined from a plot of $R_{ON}$ vs. L for devices with different channel lengths (the L-array method) with the other parameters identical using the method reported in [11]. This approach allows for $R_{SD}$ extraction without explicitly knowing the effective mobility model. The $R_{SD}$ value thus obtained is used in (9.6) to extract parameters $\theta_0$, $\gamma_0$ of unstressed device (assuming default $\Delta N_{it}$ value of $2x10^{10}cm^{-2}$ for unstressed device) using non-linear regression method with Levenberg-Marquardt algorithm [19].

After hot carrier stress, the linear on resistance of the device is modelled by (9.20), with $\Delta N_{it}$ and $R_{SD}$ as extracted parameters. Knowing the values $R_{SD}$ and $\Delta N_{it}$ for unstressed device the degradation of drain series resistance and mobility can be found. The value of extent $\delta L$ of the damaged region in (9.20) is assumed to be 0.1μm which is the approximate value width of the high field region ($1x10^5$V/cm) in the channel region obtained from simulation, as shown in Figs. 7.9 and 7.10. It should be stressed that value $\delta L$=0.1μm is an approximation and its value can vary depending on stress condition or technology. However as this region models the resistance of damaged channel region, any change in the value of $\delta L$ should reflect in the corresponding extracted $\Delta N_{it}$. The sensitivity of the extracted parameters to the variation in $\delta L$ is studied later, and it will be shown in Sec. 9.4 that a ±20% variation in the value of $\delta L$ does to significantly affect the extracted $R_{SD}$ value.

### 9.2.3 Threshold Voltage Model for Damaged Region

As pointed out in Sec. 9.2.2 due to the 2D screening effect of build in potential and applied drain voltage the threshold voltage increase for the damage $\Delta N_{it}$ in the drain region depends on the channel length, the extent $\delta L$ of the damage region as well as the value of $\Delta N_{it}$ itself.

This dependence is modelled by parameter s in expression for the threshold voltage increase ($sq\Delta N_{it}/C_{ox}$) of the damages region in (9.11). For the fixed extension of the damage region the parameter s also depends on $\Delta N_{it}$. The dependence of s on $\Delta N_{it}$ for given technology can be studied by placing a localised charge of extension 0.1μm and studying its effect on the surface potential [20].

In Figs. 9.2 and 9.3 the simulated surface potential for different $\Delta N_{it}$ placed over extension 0.1μm from the gate drain edge is shown for 2V and 5V technology devices respectively. (Since 3V technology behaves much like 2V technology, the results obtained here for 2V technology are also expected to hold true for 3V technology). It is observed that the surface potential in the damage region is not affected until a charge of $2x10^{11}cm^{-2}$ for 2V technology and $5x10^{11}cm^{-2}$ for 5V technology.

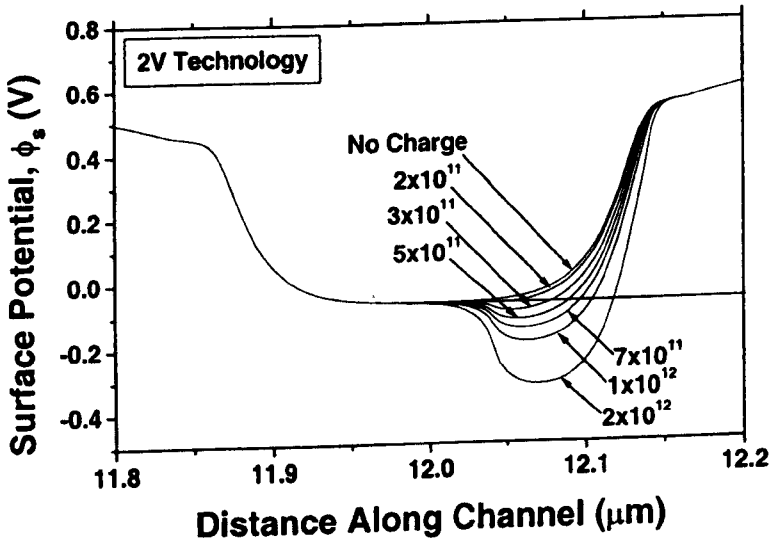


Fig. 9.2 Simulated surface potential profile for different values of interface charge placed over an extent of 0.1μm in the drain region for 2V technology.

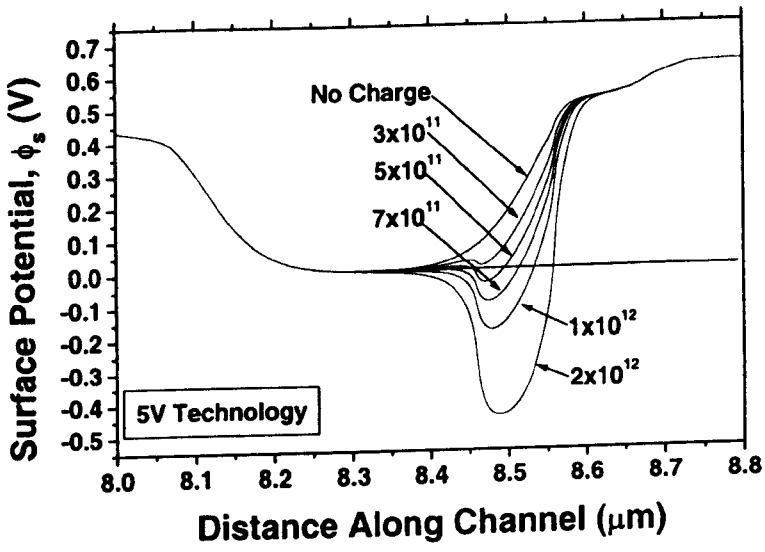


Fig. 9.3 Simulated surface potential profile for different values of interface charge placed over an extent of 0.1μm in the drain region for 5V technology.

Thus, a threshold value of $\Delta N_{it}$ exists, below which no change in the threshold voltage of the damaged region is observed. The dependence of the parameter s on $\Delta N_{it}$ for a given technology can be found by calculating ratio of change in surface potential to the maximum increase in the threshold voltage ($q\Delta N_{it}/C_{ox}$). In Fig. 9.4 the values of s as function of $\Delta N_{it}$ are shown for 2V and 5V devices. It is seen that for 2V device the value of s quickly saturates to the maximum value, while it gradually increases for 5V technology and does not saturate to the maximum value.

Since the exact functional dependence of s on $\Delta N_{it}$ is not known, it has been approximated by a step function, as illustrated in Fig. 9.4. For extracted $\Delta N_{it}$ values below the threshold, for the surface potential change s is taken as zero. After the threshold value in $\Delta N_{it}$ for the change in the surface potential is reached a constant value of s for each technology is assumed. For 2V technology a value of s~0.9 is used while for 5V technology a value of 0.5 is used.

As seen Fig. 7.4, this approximation does not significantly affects the extraction for 2V technology since the value of s quickly rises to maximum value. But an error in the extracted $\Delta N_{it}$ will be introduced for 5V technology for $\Delta N_{it}$ values in $5x10^{11}$-$1x10^{12}cm^{-2}$ range.

However as the value of s only determines increase in the channel resistance due to increase in the threshold voltage error in its value will not significantly affect the extracted $R_{SD}$.

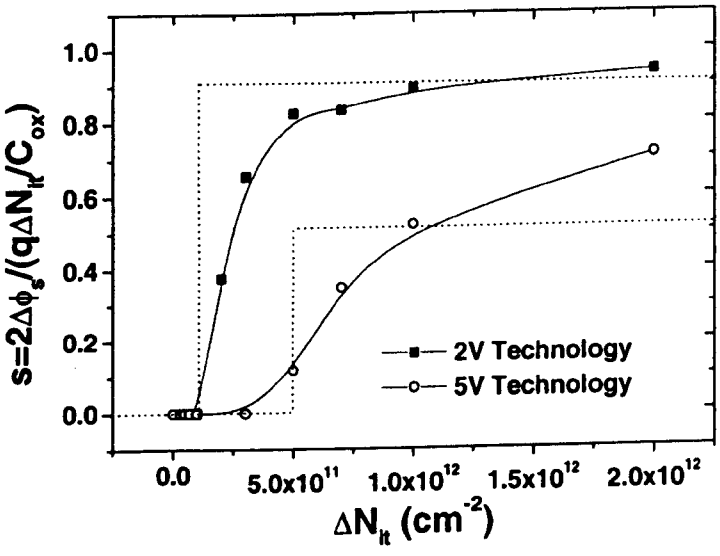


Fig. 9.4 Variation of the parameter s with interface charge for 2V and 5V technologies.

## 9.3 Parameter Extraction Using the New Methodology

The new extraction procedure developed in Sec. 9.2 is applied to extraction of series resistance and mobility degradation of 2V and 3V technologies. The results of $R_D$ and $\mu$ degradation along with corresponding experimental maximum $g_m$ degradation for 2V technology under $V_g \sim V_t$, $I_{submax}$ and $V_g=V_d$ stress conditions are shown in Figs. 9.5, 9.6 and 9.7 respectively. In Figs. 9.8, 9.9 and 9.10 the corresponding results for 3V technology device are shown.

It is seen from Figs. 9.5-9.10 that evolution of $R_D$ degradation under different stress conditions shows a consistent behaviour normally expected of graded drain devices. It is observed that $R_D$ degradation is a strong function of drain bias, and $I_{submax}$ is the worst case stress condition while the damage is lowest under $V_g=V_d$ stress condition. Further, it is seen that the mobility degradation is maximum for $I_{submax}$ condition and plays a dominant role in long-term device degradation.

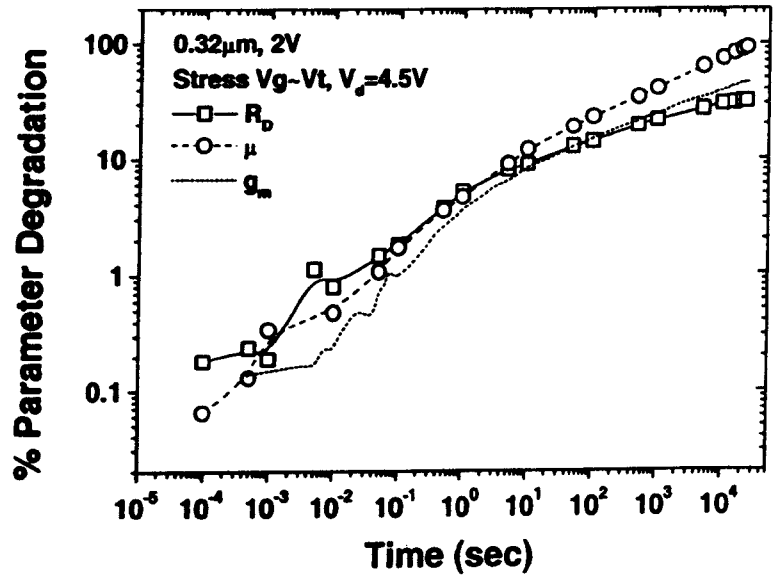


Fig. 9.5 Extracted series resistance ($R_D$), mobility ($\mu$) and experimental $g_m$ degradation for 2V technology device stressed under $V_g \sim V_t$ condition, $V_d$=4.5V.

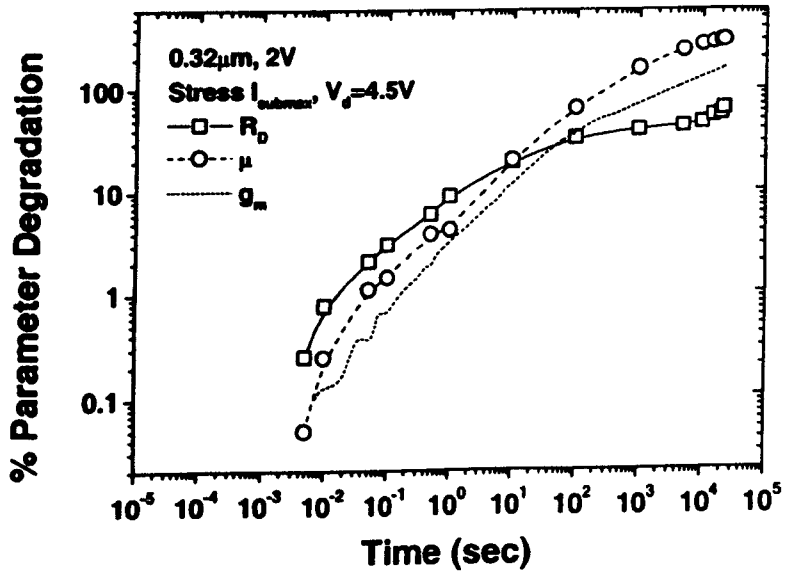


Fig. 9.6 Extracted series resistance ($R_D$), mobility ($\mu$) and experimental $g_m$ degradation for 2V technology device stressed under $I_{submax}$ condition, Vd=4.5V.

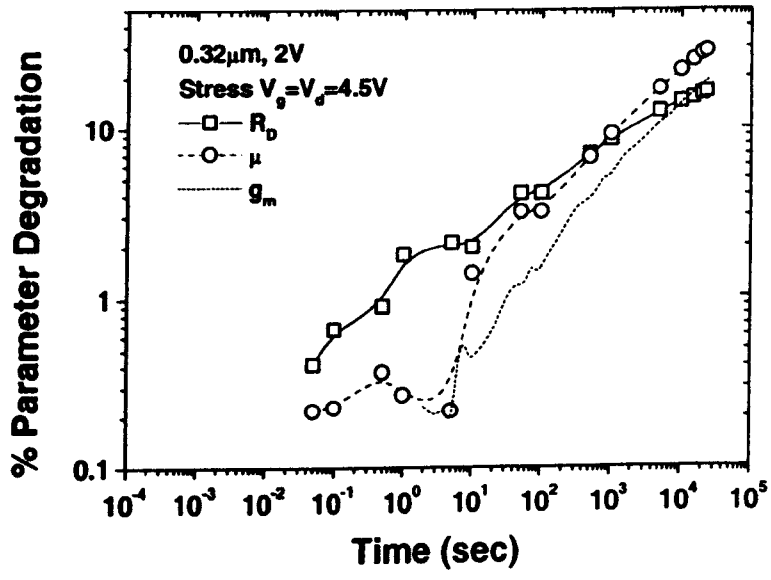


Fig. 9.7 Extracted series resistance ($R_D$), mobility (μ) and experimental $g_m$ degradation for 2V technology device stressed under condition, $V_g$=$V_d$=4.5V.

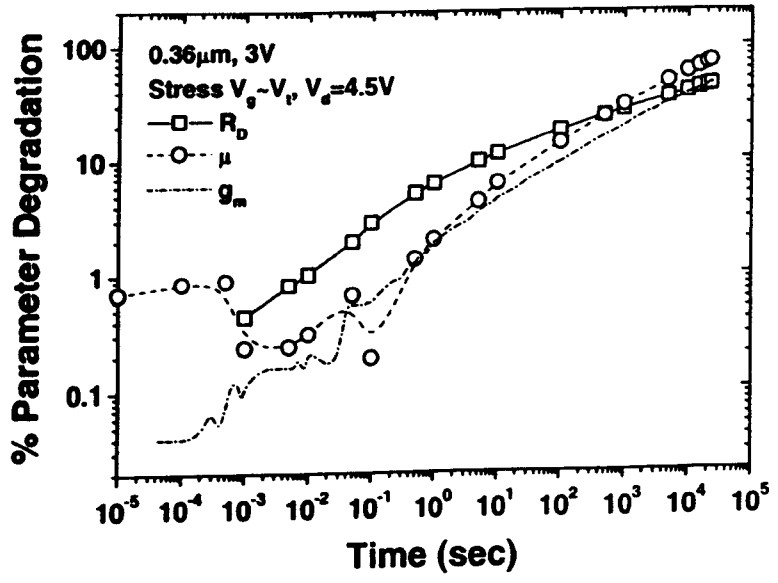


Fig. 9.8 Extracted series resistance ($R_D$), mobility (μ) and experimental $g_m$ degradation for 3V technology device stressed under $V_g$~$V_t$ condition, $V_d$=5V.

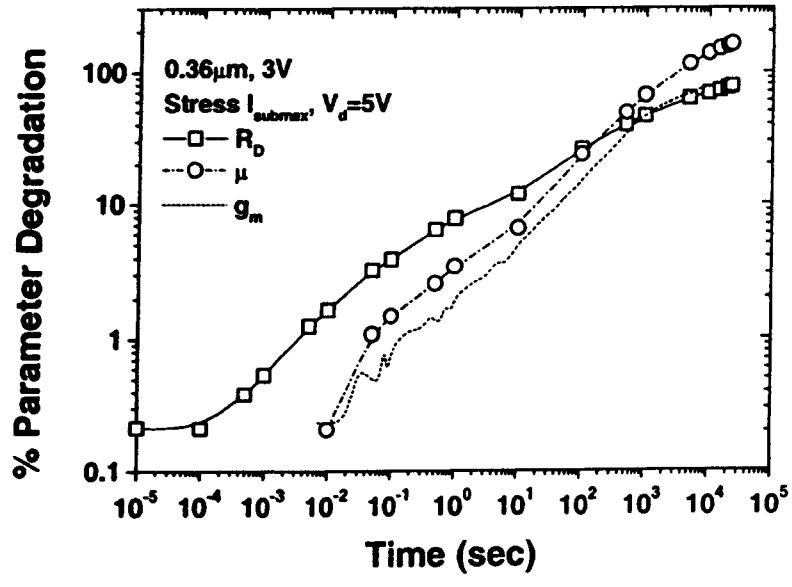


Fig. 9.9 Extracted series resistance ($R_D$), mobility (μ) and experimental $g_m$ degradation for 3V technology device stressed under $I_{submax}$ condition, Vd=5V.

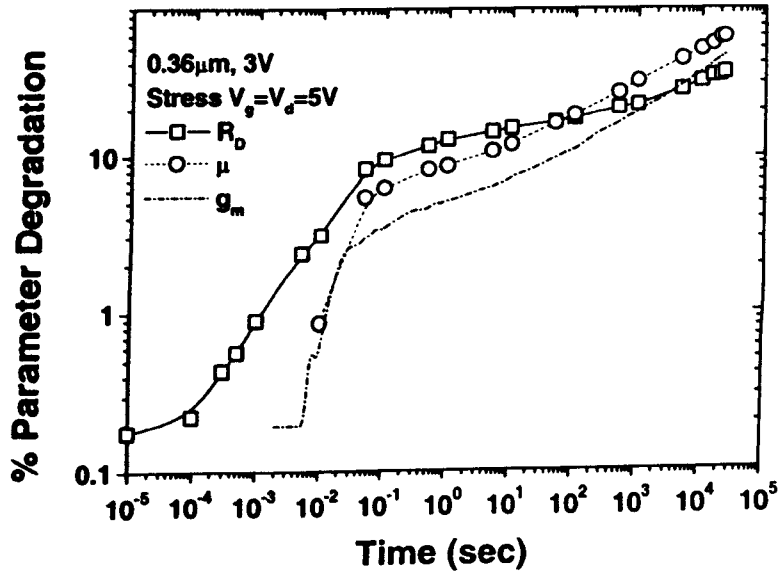


Fig. 9.10 Extracted series resistance ($R_D$), mobility (μ) and experimental $g_m$ degradation for 3V technology device stressed under $V_g$=$V_d$=5V condition.

In general, it is noted that for both 2V and 3V technologies the mobility degradation begins much earlier and strongly dominates the overall degradation behaviour as it follows $g_m$ degradation very closely. This is in contrast to 5V technology (Chapter 6) degradation behaviour where series resistance is seen to dominate and determine the $g_m$ degradation

behaviour in the early stage. This is explained by the fact that for these technologies the LDD doping is much higher which shifts the peak electric field towards the channel region (Fig. 7.10). This larger channel electric field leads to more channel damage in for short stress time causing the significant mobility degradation compared to 5V technology.

## 9.4 Sensitivity of the Methodology to Parameters α, C and δL

In this section, the stability of the new methodology to the variation in the model parameters is studied. Since parameters α and C have been empirical determined using degradation and deviation in universal mobility curves using FN stress experiments as discussed in Chapter 8, an uncertainty in their values is possible. In particular these parameters are sensitive to the calculation of the effective mobility values, which can vary for example due to variation in the device channel length or oxide thickness, as all these quantities are process sensitive. Further any error in the measurements of interface charge is an additional source of inaccuracy in the values of these parameters.

Another parameter that can affect the extracted channel and spacer damages is δL. In the extraction procedure the extent of damage region δL kept fixed for all the technologies and under different stress condition. However, in practice small variation in δL from one technology to another or one stress conditions to another is expected. Further a variation in δL as function stress time is possible. Both of these factors are expected to contribute to an error in the extracted damage after stress.

It is therefore important to quantify the sensitivity of the model parameters to extracted interface charge ($\Delta N_{it}$) and series resistance $R_{SD}$. This is achieved by allowing a ± 20% variation in the parameters α, C and δL and studying the variation the extracted values of $\Delta N_{it}$ and $R_{SD}$ compared with normally obtained values for a fixed stress time. The normal values of extracted parameters here refer to the values obtained with the parameters α, C and δL used in Sec. 9.3 above. Tables 9.1, 9.2 and 9.3 compares the variation in the extracted parameters with the normally obtained values for 2V technology device stressed under $I_{submax}$ conditions (worst case damage), $V_d$=4.5V after 1000s stress time. The percentage variation in the extracted $\Delta N_{it}$ and $R_{SD}$ with respect to the normal values is also indicated in the parenthesis of the each parameter variation.

Table 9.1

| Parameter α | $\Delta N_{it}(cm^{-2})$ | $R_{SD}$ (Ω) |
|---|---|---|
| Normal | $2.94x10^{12}$ | 27.352 |
| +20% Variation | $2.738 x10^{12}$ (-6.87%) | 25.98 (-5.01%) |
| -20% Variation | $3.196x10^{12}$ (8.5%) | 29.35 (7.35%) |

Table 9.2

| Parameter C | $\Delta N_{it}(cm^{-2})$ | $R_{SD}$ (Ω) |
|---|---|---|
| Normal | $2.94x10^{12}$ | 27.352 |
| +20% Variation | $2.935 x10^{12}$ (-0.17%) | 27.834(1.75%) |
| -20% Variation | $2.966x10^{12}$ (0.88%) | 26.413 (-3.42%) |

Table 9.3

| Parameter δL | $\Delta N_{it}(cm^{-2})$ | $R_{SD}$ (Ω) |
|---|---|---|
| Normal | $2.94x10^{12}$ | 27.352 |
| +20% Variation | $2.647 x10^{12}$ (-9.96%) | 27.26 (-0.31%) |
| -20% Variation | $3.31x10^{12}$ (12.5%) | 27.59 (0.87%) |

It is observed from Table 9.1 and 9.2 that for the parameters α and C a ± 20% variation results in less that 10% variation in extracted $\Delta N_{it}$ and $R_{SD}$. This shows that the method is

indeed robust with respect to variation in $\alpha$ and C, allowing for a significant tolerance in any error in their values. For the variation in parameter $\delta L$, it is noted from Table 9.3 that the extracted series resistance is insensitive to its variation. This also physically justifies the approach used. Since, in this approach the damage in channel region is replaced be equivalent uniform damage of extent $\delta L$, any variation the $\delta L$ is expected only to change the values of channel damage $\Delta N_{it}$, which is seen to vary by nearly 10%. On the other hand, the damage in the spacer region is only modelled by increase in $R_{SD}$, which should be independent of the extent of damage in the channel region.

## 9.4 Verification of the New Procedure

### 9.4.1 Transconductance

Manipulating (9.20) $R_{ON}$ can be expressed as

$$R_{ON}=\frac{\left(\begin{array}{l}\frac{L_0}{L}(V_{gs}-V_{t0}-\delta V-V_{ds2}/2)\left(1+\theta_0(V_{gs}+V_{t0}-V_{ds1}/2)^{\gamma 0}\right)+\\ \frac{\delta L}{L}(1+\alpha\Delta N_{it})(V_{gs}-V_{t0}-V_{ds1}/2)\left(1+\theta_0 e^{-C\Delta Nit}(V_{gs}+V_{t0}-\delta V-V_{ds2})^{\gamma_0}\right)+\\ \frac{\mu_0 C_{ox} W}{L}R_{SD}(V_{gs}-V_{t0}-\delta V-V_{ds2}/2)(V_{gs}-V_{t0}-V_{ds1}/2)\end{array}\right)}{\frac{\mu_0 C_{ox} W}{L}(V_{gs}-V_{t0}-\delta V-V_{ds2}/2)(V_{gs}-V_{t0}-V_{ds1}/2)} \tag{9.21}$$

where $V_{ds1}=(V_{ds}-V^{''}_{ds})/2$, $V_{ds2}=(V_{ds}+V^{'}_{ds})/2$ and $\delta V=sq\Delta N_{it}/C_{ox}$. The linear region drain current can from $I_{ds}=V_{ds}/R_{ON}$, giving

$$I_{ds}=\frac{\beta_0(V_{gs}-V_{t0}-\delta V-V_{ds2}/2)V_{ds}}{\left(\begin{array}{l}\frac{L_0}{L}\left(\frac{V_{gs}-V_{t0}-\delta V-V_{ds2}/2}{V_{gs}-V_{t0}-V_{ds1}/2}\right)\left(1+\theta_0(V_{gs}+V_{t0}-V_{ds1}/2)^{\gamma 0}\right)+\\ \frac{\delta L(1+\alpha\Delta N_{it})}{L}\left(1+\theta_0 e^{-C\Delta Nit}(V_{gs}+V_{t0}-\delta V-V_{ds2})^{\gamma_0}\right)+\beta_0 R_{SD}(V_{gs}-V_{t0}-\delta V-V_{ds2}/2)\end{array}\right)} \tag{9.22}$$

where $\beta_0=\mu_0 C_{ox} W/L$. The other parameters have similar meaning as in (9.20). Differentiating (9.22) with respect to $V_{gs}$ gives transconductance $g_m$.

The measured $g_m$ degradation obtained directly from $I_{ds}$-$V_{gs}$ characteristics and $g_m$ degradation calculated by differentiating (9.22) are compared as function stress time. Figs. 9.11 and 9.12 show the results of measured and calculated $g_m$ degradation for 2V and 3V technology devices, as a function of stress time for $I_{submax}$ stress condition (similar fits are observed for other stress conditions, not shown here). It is sees that measured and calculated values match to within 2-3% of variation. The excellent agreement between calculated and measured $g_m$ degradations demonstrates the ability of the new methodology to accurately calculate the affect of channel and spacer damages on the degradation of device parameters.

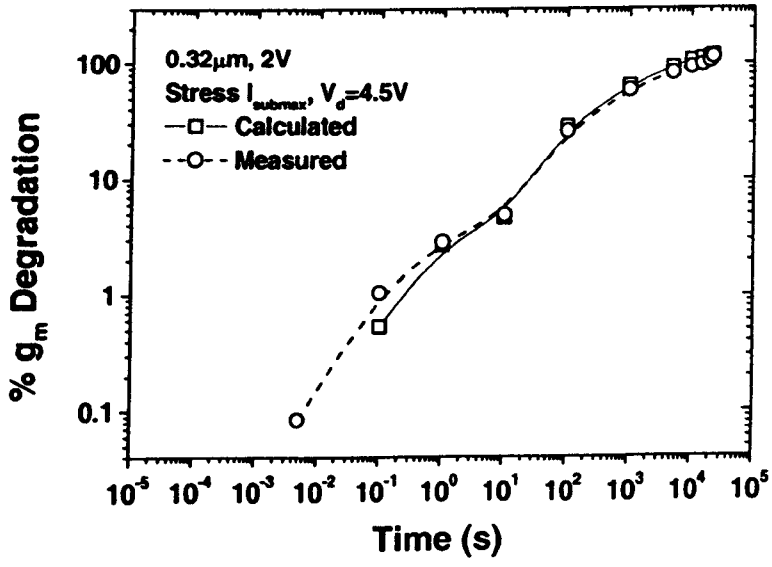


Fig. 9.11 Comparison of measured and calculated values of $g_m$ degradation (using (9.22)) under $I_{submax}$ stress condition, $V_d$=4.5V for 2V technology device.

### 9.4.2 Correlation of Extracted Series Resistance Degradation with Simulation

In order to validate the physical plausibility of the extracted $R_D$ degradation using the new methodology, the numerical simulation predicting the dependence of $R_D$ increase on the charge in the spacer region are used. Although a direct correlation between experiments and simulations cannot be obtained from the present measurements, since that will require knowledge of time evolution of charge generation ($\Delta N_{itsp}$) in the spacer region. This procedure for verification of the extracted $R_D$ degradation relies on establishing that the

saturating series the $R_D$ increase seen in Sec. 9.3 is due to saturating behaviour of $\Delta N_{itsp}$ generation. For demonstration 2V technology is used.

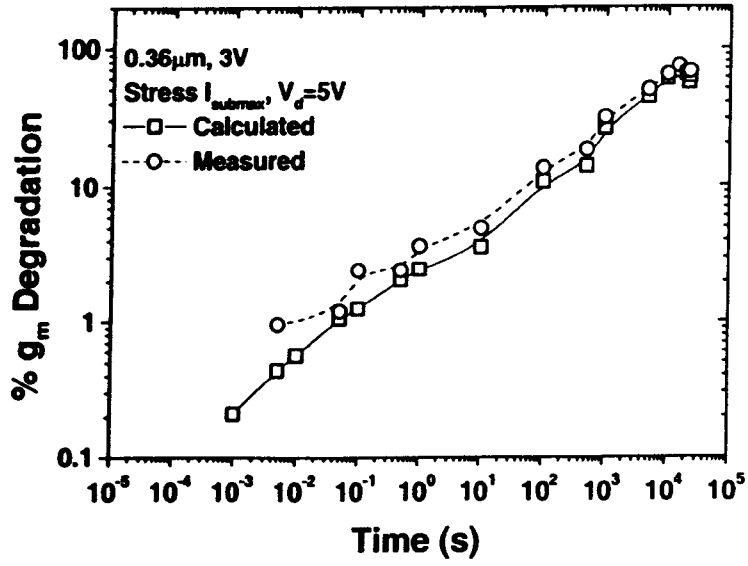


Fig. 9.12 Comparison of measured and calculated values of $g_m$ degradation (using (9.22)) under $I_{submax}$ stress condition, $V_d$=5V for 3V technology device.

In this approach the increase in $R_D$ as a function $\Delta N_{itsp}$ is obtained by 2D device simulator MEDICI and a comparison is made with experimentally obtained values to obtain a correlation between the charge in the spacer region and experimental stress time. In the simulations series source-drain resistance as function of the gate bias is calculated from the heat dissipated in source-drain regions of the device. It has been reported that for LDD n-MOSFETs heat dissipated by carrier transport is predominantly caused by Joule heating, while contribution of Thompson heat and recombination heat can be neglected [20]. The Joule heat can be expressed as [21]

$$H_J = \rho_n \vec{J}_n \cdot \vec{J}_n + \rho_p \vec{J}_p \cdot \vec{J}_p \qquad (9.23)$$

where $\rho_n$ and $\rho_p$ electron and hole resistivities, $\vec{J}_n$ and $\vec{J}_p$ are electron and hole current densities. For LDD n-MOSFET electrons are the majority carriers and only first term on the right hand side of (9.23) is important. So, the total series source-drain resistance can be written as volume integration over source drain regions of first term in (9.23)

$$R_{SD}(V_{gs}) = \frac{\int \rho_n \vec{J}_n \cdot \vec{J}_n dV}{I_{ds}^2} \qquad (9.24)$$

In order to evaluate the integral in (9.24), the device is simulated for a fixed gate bias in the linear region of operation extracting product $\rho_n \vec{J}_n \cdot \vec{J}_n$, which is then numerically integrated over source drain regions. In Fig. 9.13 $R_{SD}(V_{gs})$ curves obtained by this procedure for different quantities of $\Delta N_{itsp}$ in spacer region are shown. In the simulations the width of spacer region over which $\Delta N_{itsp}$ is placed is 200Å which is determined from simulated electric field profile under the spacer region shown in Fig. 7.10. It is observed that $R_{SD}$ decreases with the gate voltage due to the gate voltage dependence of accumulation layer and spreading resistances. The effect of negative charge in the spacer region on current conduction in the LDD region is twofold. Firstly, it increases resistivity $\rho_n$ of drain region under the spacer due to depletion of underlying LDD $n^-$ layer and secondly the increase in product $\vec{J}_n \cdot \vec{J}_n$ due to current crowding caused by repulsion of current flow lines from the surface into the bulk. Thus leading to increase $R_{SD}$ with the charge in spacer region.

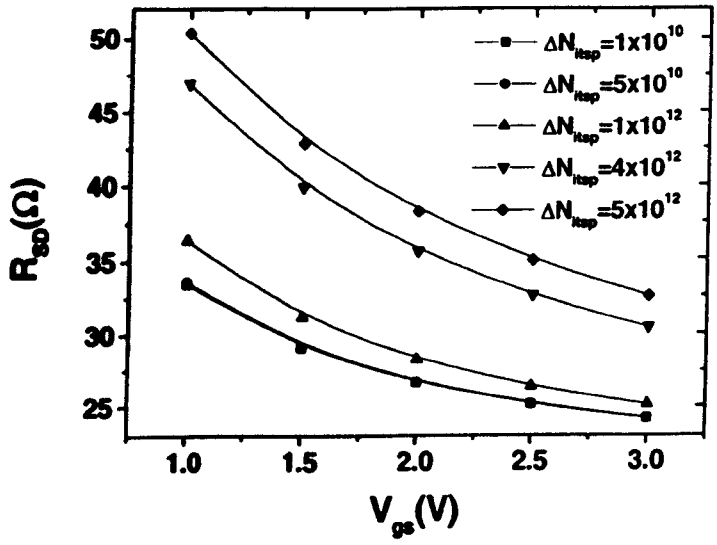


**Fig.9.13 Series source drain resistance ($R_{SD}$) as function of the gate voltage for different values of interface charge ($\Delta N_{itsp}$ in $cm^{-2}$) placed in the spacer region for 2V technology device.**

Since series resistance is gate voltage dependent, $R_{SD}$ model proposed in [16] is used

$$R_{SD}(V_{gs}) = R_{SD} + \frac{a}{V_{gs} - V_t - V_{ds}/2} \tag{9.25}$$

where parameter a is approximately taken as $\Delta L/\mu_0 C_{ox} W$ and for sake of simplicity its dependence on the gate voltage is ignored. In Fig. 9.14 the increase in $R_D$ obtained as function of $\Delta N_{itsp}$ is shown. It is seen that $R_D$ increases almost linearly for low $\Delta N_{itsp}$ values but deviates from linear behaviour at high $\Delta N_{itsp}$ values. This dependence of $R_D$ increase on $\Delta N_{itsp}$ can be explained by considering following first order analytic expression for $R_D$ [6] (here contribution of contact and metal resistance etc. has been excluded)

$$R_D = \frac{L_{ldd}}{qW\mu_n Q_n} \tag{9.26}$$

where $L_{ldd}$ is the effective length of the LDD region and $Q_n$ effective sheet concentration of free carriers in drain region which is determined by LDD doping.

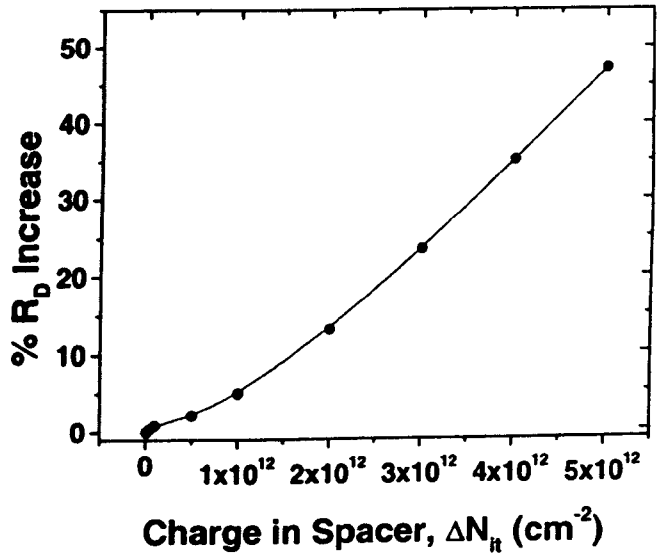


Fig. 9.14 Percentage increase in drain series resistance as a function of charge in the spacer region obtained from fitting model (9.25) to numerically extracted series resistance.

Assuming that after hot carrier stress interface region of extension $\Delta L_d$ in the drain spacer is damaged, increase in $R_D$ can be obtained from (9.26) as

$$\Delta R_D = \frac{\Delta L_d}{qW\mu_n(Q_n - \Delta N_{itsp})} + \frac{L_{unstressed}}{qW\mu_n Q_n} - \frac{\Delta L_d + L_{unstressed}}{qW\mu_n Q_n} \tag{9.27}$$

where $L_{unstressed}$ is the length of unstressed LDD region, and $\Delta N_{itsp}$ is the increase in interface states in the damaged region. After simple algebraic manipulation (9.27) can be written as

$$\Delta R_D = \frac{\Delta L_d}{qW\mu_n Q_n}\left[\left(\frac{\Delta N_{itsp}}{Q_n}\right) + \frac{1}{2}\left(\frac{\Delta N_{itsp}}{Q_n}\right)^2 + O(x)\right] \tag{9.28}$$

where term O(x) refers to higher order terms in power series expansion of $1/(1-\Delta N_{itsp}/Q_n)$. For values $(\Delta N_{it}/Q_n) << 1$ it is seen from (9.28) that $\Delta R_D$ increases linearly with $\Delta N_{itsp}$. But for large spacer charge second and higher order terms in (9.28) become important and relation between $\Delta R_D$ and $\Delta N_{itsp}$ in general becomes non-linear as seen in Fig. 9.14. Thus it is noted from Fig. 9.14 that by assigning interface charge in spacer region the increase in $R_D$ from simulation can be matched to experimentally obtained values. For example in order to obtain 20% increase in $R_D$ obtained after 1000s, for the device stressed under $I_{submax}$ condition (Fig. 9.5) $\Delta N_{itsp}$ values of $2.5\times10^{12}cm^{-2}$ from Fig. 9.14 are required to be generated.

From (9.28) it is noted that to a first order increase in $R_D$ is directly proportional to $\Delta N_{itsp}$, so for experimentally obtained $R_D$ degradation the time evolution of $\Delta N_{itsp}$ increase should follow $R_D$ degradation behaviour seen in Figs. 9.5-9.7. In order to confirm this dependence the values of $R_D$ degradation for different stress conditions in Figs. 9.5-9.7 are matched for the same values obtained using simulation in Fig. 9.14, and the corresponding $\Delta N_{itsp}$ from Fig. 9.14 and stress time in Figs. 9.5-9.7 are obtained. In Fig. 9.15, $\Delta N_{itsp}$ degradation as a function of the stress time obtained using this approach are shown for $V_g \sim V_t$, $I_{submax}$ and $V_g = V_d$ stress conditions.

A very good similarity between $R_D$ and $\Delta N_{itsp}$ degradation behaviours with the stress time in Figs. 9.5-9.7 and 9.15 is seen. This shows that saturating $R_D$ degradation characteristic points to saturating behaviour of generated charge in the spacer region. Further since this correlation between $R_D$ and $\Delta N_{itsp}$ degradation has been obtained by assuming physically based $R_D$ degradation model (9.28), the correlation in Fig. 9.15 also gives an indirect validation of the extracted $R_D$ degradation behaviour using the new methodology.

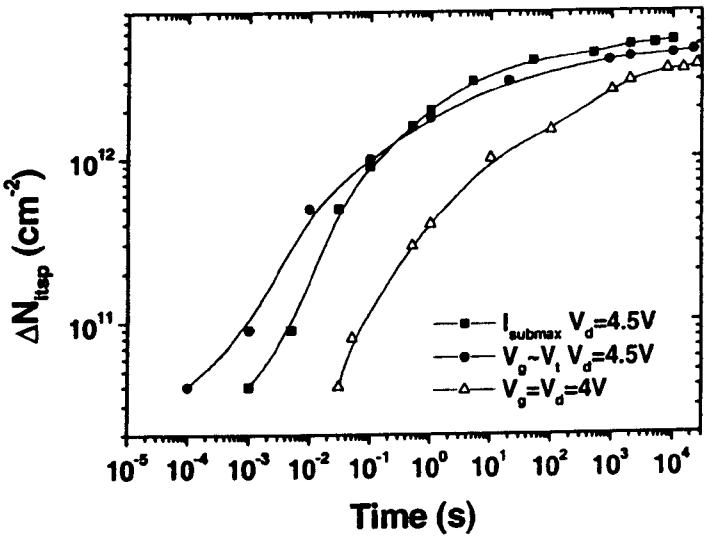


Fig. 9.15 Correlated increase in interface states ($\Delta N_{itsp}$) from Fig. 9.14 and time from Figs. 9.5-9.7.

### 9.4.3 Threshold Voltage

The shift in the threshold voltage extracted using linear extrapolation method has been commonly used to obtain the information about the damage [22], [23]. The application of this extraction method is based on the assumption that well-known linear region I-V model for a MOSFET (Eq. 2.21) is applicable to a hot carrier stressed device like for the case of the uniformly damaged MOSFET (e. g. FN stressed device). Although the changes in $V_t$ obtained in this manner gives an indication of the nature of the damage, i. e. positive shift indicative of the negative oxide charge and negative shift indicative of the positive charge. But the amount of the change in $V_t$ is not a direct measure of the amount of the oxide charge generated. Since the hot carrier damage is non-uniform, the calculation $V_t$ from extracted channel damage after stress and its correlation to experimentally extracted $V_t$ is not straightforward.

For unstressed or uniformly stressed device the conventional definition of $V_t$ corresponds to the gate voltage when surface potential in the channel region is $2\phi_B$, which has a unique value. However this definition losses a great deal of physical meaning for hot carrier stressed device. As discussed in Sec. 9.2.3 in this case the device will turn on when the gate voltage is such that the minimum surface potential of $2\phi_B$ in the damaged region is reached. Since the undamaged region of the channel will turn on before the damaged region, there are in effect two threshold voltages. Consequently, for a particular gate voltage the inversion layer charge

in the damaged and undamaged region are different determined by their respective threshold voltages.

Because of this non-uniform damage the threshold voltage change of the damaged region (modelled as $sq\Delta N_{it}/C_{ox}$ in Sec. 9.2.2) is in general different from the change in equivalent threshold voltage extracted using conventional linear region I-V model. Fig. 9.16 compares the linearly extracted $V_t$ after stress with the calculated $V_t$ of the damaged region for 2V device stressed under $I_{submax}$ condition. The threshold voltage for the damage region is defined as: $V_t=V_{t0}+ sq\Delta N_{it}/C_{ox}$. It is noted that at a given stress time the calculated $V_t$ of the damaged region is higher than extracted $V_t$. Results of simulations on 2V device using MEDICI under similar condition as for the experimental device shown in Fig. 9.17 also confirm this difference. In simulations the calculated and linearly extracted $V_t$ are obtained for different interface charge placed over 0.1μm extension for 2V technology. From Fig. 9.17, it is observed that the extracted $V_t$ for a given amount of the damage (for s>0) is lower than the calculated $V_t$ of the damaged region.

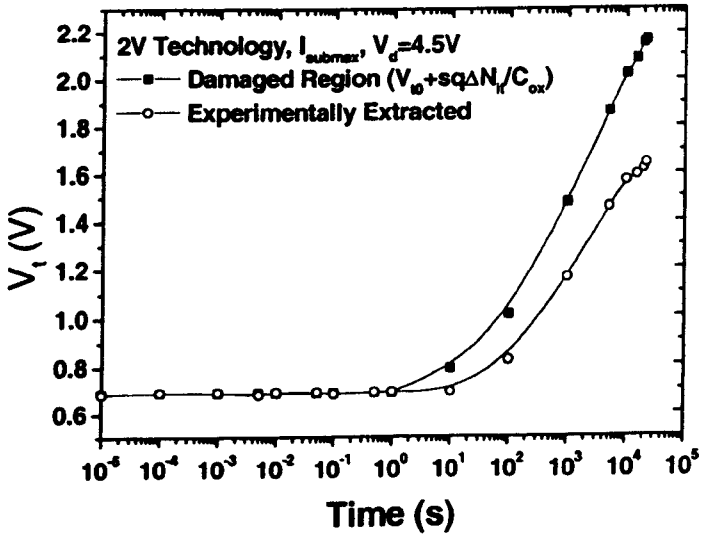


Fig. 9.16 Comparison of the threshold voltage of the damaged region with the experimentally extracted threshold voltage.

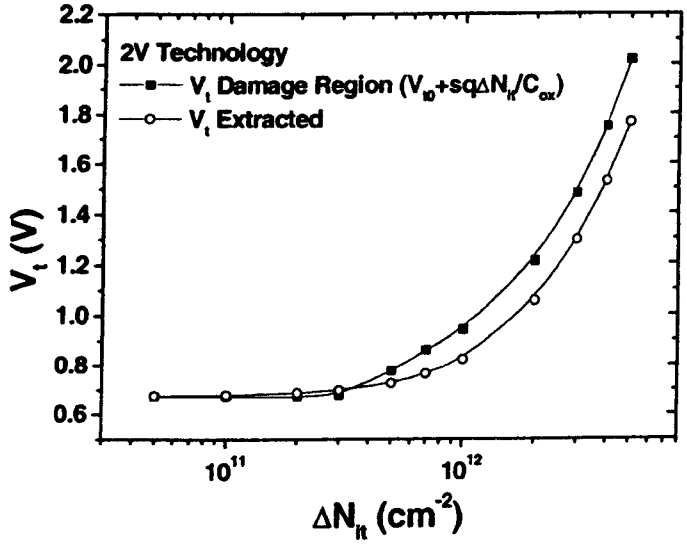


Fig. 9.17 Comparison of the calculated and extracted threshold voltages using simulations, the extent of the damaged region over which the charge is placed from the gate-drain edge towards channel is 0.1μm.

In order to arrive at a generalised analytic threshold voltage model for non-uniformly stressed device, it desired to formulate the linear region drain current model at the onset of inversion considering the on resistance models of the damaged and undamaged regions. Such a case for very small threshold voltage change has been suggested in [24]. As discussed in Secs. 9.2.1 and 9.2.2 the linear region resistance of undamaged and damaged channel regions is determined by their respective threshold voltages. Since for the gate voltages near $V_t$ the channel resistance is 3 to 4 orders of magnitude higher than the series resistance. The contribution of the series resistance to the total on resistance of the device in this region of the operation can be ignored. The on resistance of the stressed device can then be expressed, using (9.8) and (9.11), as sum of resistances of damaged region of length δL and undamaged region of length $L_0$

$$R_{ON} = \frac{L_0}{\mu_{eff} C_{ox} W(V_{gs} - V_{t0})} + \frac{\delta L}{\mu'_{eff} C_{ox} W(V_{gs} - V_t)} \tag{9.29}$$

where $\mu_{eff}$ is the effective mobility of the undamaged region and $\mu'_{eff}$ is the effective mobility in the damaged region. In (9.29) since terms $V_{ds}$, $V'_{ds}$ $V''_{ds}$ are constant and are very small compared to threshold voltage, for sake of simplicity $V_{t0}$~$V_{t0}$ +1/2($V_{ds}$-$V''_{ds}$) and $V_t$~$V_{t0}$+

$sq\Delta N_{it}/C_{ox}+1/2(V_{ds}+V'_{ds})$ have been taken. As the vertical field at the onset of the channel formation is small, so by definition the linear region $V_t$ does not account for the variation of effective mobility with the gate voltage as well as its reduction due to interface charge. Therefore the effective mobility of the damaged and undamaged channel regions can be approximated as constant $\mu_0$, thus $\mu_{eff}$ and $\mu'_{eff}$ in (9.29) can be replaced by $\mu_0$. Defining $I_{ds}=V_{ds}/R_{ON}$, the linear region current from (9.29) can be written as

$$I_{ds}=\frac{\mu_0 C_{ox} W(V_{gs}-V_{t0})(V_{gs}-V_t)}{\delta L(V_{gs}-V_{t0})+L_0(V_{gs}-V_t)}V_{ds} \tag{9.30}$$

Eq. (9.30) can be further simplified by letting $V_t=V_{t0}+\delta V$

$$I_{ds}=\frac{\mu_0 C_{ox} W(V_{gs}-V_t)V_{ds}}{(L_0+\delta L)\left[1-A\dfrac{\delta V}{(V_{gs}-V_{t0})}\right]} \tag{9.31}$$

where $\delta V$ is the change in the threshold voltage of the damaged channel region and $A=L_0/(L_0+\delta L)$. Eq. (9.31) implies that as long as the device can be turned on, the second term in the square brackets in the denominator is less than one. Expanding the dominator term in (9.31) as power series $1+x+x^2+x^3+\ldots$, $I_{ds}$ can be expressed as

$$I_{ds}=\frac{\mu_0 C_{ox} W}{(L_0+\delta L)}(V_{gs}-V_{t0}-\delta V)\left\{\begin{array}{l}1+A\dfrac{\delta V}{(V_{gs}-V_{t0})}+A^2\dfrac{\delta V^2}{(V_{gs}-V_{t0})^2}+A^3\dfrac{\delta V^3}{(V_{gs}-V_{t0})^3}+\\ A^4\dfrac{\delta V^4}{(V_{gs}-V_{t0})^4}+\ldots\end{array}\right\}V_{ds} \tag{9.32}$$

Carrying out the multiplication in (9.32) $I_{ds}$ can be expressed as,

$$I_{ds}=\frac{\mu_0 C_{ox} W}{(L_0+\delta L)}\left\{\begin{array}{l}(V_{gs}-V_{t0}-\delta V)\left\{1+A\dfrac{\delta V}{(V_{gs}-V_{t0})}\right\}+A^2(V_{gs}-V_{t0}-\delta V)\dfrac{\delta V^2}{(V_{gs}-V_{t0})^2}+\\ A^3(V_{gs}-V_{t0}-\delta V)\dfrac{\delta V^3}{(V_{gs}-V_{t0})^3}+A^4(V_{gs}-V_{t0}-\delta V)\dfrac{\delta V^4}{(V_{gs}-V_{t0})^4}+\ldots\end{array}\right\}V_{ds}$$

(9.33)

By algebraic manipulation it can be shown that the first product on the right hand side of (9.33) is

$$(V_{gs} - V_{t0} - \delta V)\left(1 + A\frac{\delta V}{(V_{gs} - V_{t0})}\right) = V_{gs} - \left(\frac{L_0 V_{t0} + \delta L V_t}{L_0 + \delta L} + A\frac{\delta V}{(V_{gs} - V_{t0})}\right) \tag{9.34}$$

Substituting (9.34) into (9.33) and computing the rest of the products, and rearranging (9.33) becomes

$$I_{ds} = \frac{\mu_0 C_{ox} W}{(L_0 + \delta L)}\left[V_{gs} - \left(\frac{L_0 V_{t0} + \delta L V_t}{L_0 + \delta L} + (1 - A)\left(\begin{array}{l} A\dfrac{\delta V^2}{(V_{gs} - V_{t0})} + A^2\dfrac{\delta V^3}{(V_{gs} - V_{t0})^2} + \\ A^3\dfrac{\delta V^4}{(V_{gs} - V_{t0})^3} + A^4\dfrac{\delta V^5}{(V_{gs} - V_{t0})^4} + \ldots \end{array}\right)\right)\right]V_{ds} \tag{9.35}$$

For small damage the term $\delta V$ in (9.35) is very small and its second and higher order terms can be ignored simplifying (9.35) to

$$I_{ds} = \frac{\mu_0 C_{ox} W}{(L_0 + \delta L)}\left[V_{gs} - \left(\frac{L_0 V_{t0} + \delta L V_t}{L_0 + \delta L}\right)\right]V_{ds} \tag{9.36}$$

Thus for small $\delta V$ the linearly extrapolated threshold voltage can be approximated by [24]

$$V_{tlin} = \frac{L_0 V_{t0} + \delta L V_t}{L_0 + \delta L} \tag{9.37}$$

However when term $\delta V$ is large, as is the case for severely stressed device where $\delta V$ can reach one or more, the second and higher order terms in (9.35) also become important and the linearly extrapolated threshold voltage takes a generalised form

$$V_{tlin} = \frac{L_0 V_{t0} + \delta L V_t}{L_0 + \delta L} + (1-A)\left( A\frac{\delta V^2}{(V_{gs}-V_{t0})} + A^2\frac{\delta V^3}{(V_{gs}-V_{t0})^2} + A^3\frac{\delta V^4}{(V_{gs}-V_{t0})^3} + A^4\frac{\delta V^5}{(V_{gs}-V_{t0})^4} + \ldots \right) \quad (9.38)$$

Taking common the term $A\delta V^2/(V_{gs}-V_{t0})$ in the infinite sum in (9.38), $V_{tlin}$ can be expressed as

$$V_{tlin} = \frac{L_0 V_{t0} + \delta L V_t}{L_0 + \delta L} + A(1-A)\frac{\delta V^2}{V_{gs}-V_{t0}}\left( 1 + A\frac{\delta V}{(V_{gs}-V_{t0})} + A^2\frac{\delta V^2}{(V_{gs}-V_{t0})^2} + A^3\frac{\delta V^3}{(V_{gs}-V_{t0})^3} + \ldots \right) \quad (9.39)$$

The infinite product in round brackets in (9.39) is infinite series $1 + x + x^2 + x^3 + \ldots = 1/(1-x)$, with $x = A\delta V/(V_{gs}-V_{t0})$. Replacing this sum in (9.39) by $1/[1 - A\delta V/(V_{gs}-V_{t0})]$, $V_{tlin}$ can be expressed as

$$V_{tlin} = \frac{L_0 V_{t0} + \delta L V_t}{L_0 + \delta L} + \frac{(1-A)A\delta V^2}{V_{gs} - V_{t0} - A\delta V} \quad (9.40)$$

From (9.40), it is seen that the linearly extracted threshold voltage itself depends on the range of gate voltage bias values used, decreasing with increasing gate voltage at which the straight line on $I_{ds}$-$V_{gs}$ curve is fitted. As the linearly extrapolated threshold voltage in the measurements is found by extrapolating to zero gate voltage the straight line fitted to $I_{ds}$-$V_{gs}$ curves at point of maximum slope of $I_{ds}$-$V_{gs}$ (maximum $g_m$). An upper bound for the threshold voltage can be approximated by letting $V_{gs}$ in (9.40) equal to the gate voltage value, $V_{gmax}$, at which maximum $g_m$ is found. Thus letting $V_{gs} = V_{gmax}$ in (9.40), the threshold voltage can be expressed as

$$V_{tlin} = \frac{L_0 V_{t0} + \delta L V_t}{L_0 + \delta L} + \frac{(1-A)A\delta V^2}{V_{gmax} - V_{t0} - A\delta V} \quad (9.41)$$

where in (9.41) the value of $V_{gmax}$ is found from point of maximum experimental $g_m$ after every stress period. Figs. 9.18 and 9.19 show experimental and calculated, using (9.41), threshold voltages for 2V device stressed and 3V device stressed under $I_{submax}$ stress condition

respectively. In Figs. 9.18-9.19 the first order calculated threshold voltages, (9.37), ignoring higher order terms in $\delta V$ is also shown for comparison.

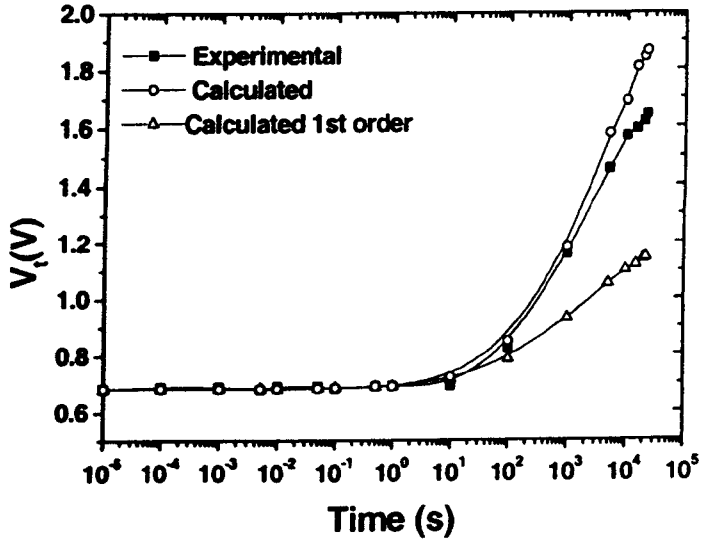


Fig. 9.18 Comparison of the $V_t$ calculated using model (9.41) and experimentally measured threshold voltage for 2V device stressed under $I_{submax}$, $V_d$=4.5V stress condition. $V_t$ calculated using 1st order approximation (9.37) is also shown.

A good agreement between measured and calculated $V_t$ degradation is observed in Figs. 9.18 and 9.19 and worst case calculated and measured $V_t$ matches to an accuracy of within 13%. This validates the extraction procedure and the approximation used in deriving the $V_t$ model. It is noted that for low values of threshold voltage increase ($\delta V <= 0.1$) the first order expression for $V_t$ (9.37) also gives good match to the experimental values. A deviation between experimental and calculated $V_t$ for large stress time for 2V device (worst case damage) is observed in Fig. 9.18. It is seen in Fig. 9.18 that the experimental $V_t$ for large stress time is lower that the calculated $V_t$. This difference could be due to an increase in the value of $\delta L$ under very high stress, after long stress time. Since the extracted $\Delta N_{it}$ is obtained by assuming $\delta L$ as fixed, any increase in $\delta L$ with stress time will result in lower $\Delta N_{it}$ and will give better match to the experimental $V_t$.

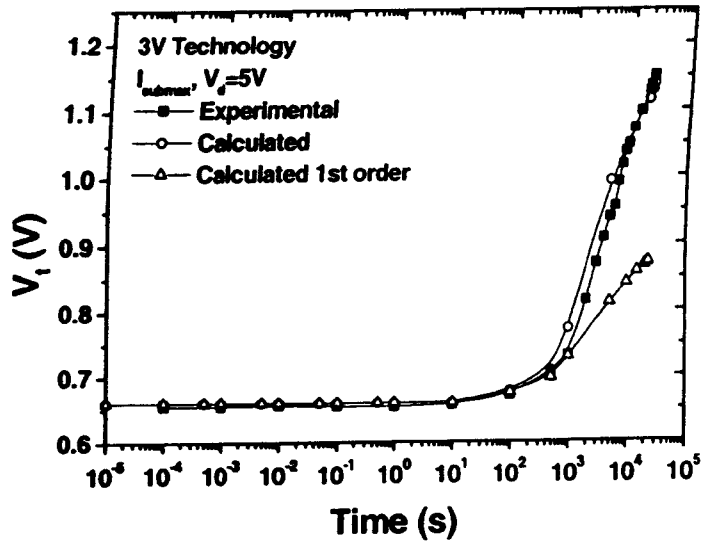


Fig. 9.19 Comparison of the $V_t$ calculated using model (9.41) and experimentally measured threshold voltage for 3V device stressed under $I_{submax}$ $V_d$=4.5V stress condition, $V_t$ calculated using 1st order approximation (9.37) is also shown.

As a further validation of the extracted channel damage using the new model the experimentally extracted $V_t$ is compared with simulation. In order to achieve this, the channel damage ($\Delta N_{it}$) extracted using the new method under $I_{submax}$ stress condition for 2V device is used. The extracted values of the channel damage using the new methodology ($\Delta N_{it}$) are correlated with the corresponding stress time to obtain experimental $V_t$ degradation as function of $\Delta N_{it}$. In the simulation localised charge of similar values as extracted $\Delta N_{it}$ from experimental data is placed in the drain region with extension of 0.1μm. The device is then simulated in the linear region ($V_{ds}$=0.1) and linear $V_t$ is extracted. Fig. 9.20 shows $V_t$ comparison of experimental and simulated values along with $V_t$ model (9.41).

It is seen in Fig. 9.20 that the agreement between the experiment and simulation is good, although the worst-case experimental $V_t$ is 10% lower than simulated $V_t$. This difference could be attributed to the fact that in experiments the damage is actually non-uniform which has been approximated by equivalent uniform damage in the extraction. It is expected that the amount of change in $V_t$ due to non-uniform damage will be lower than the equivalent uniform damage due to dependence of the screening parameter on $\Delta N_{it}$.

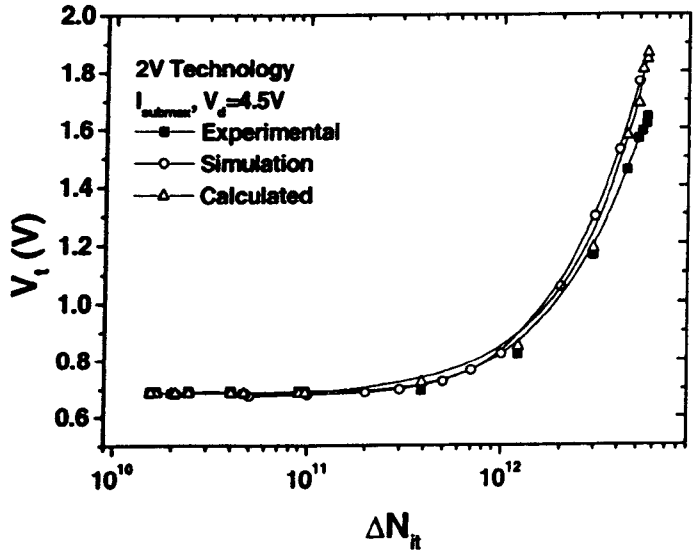


Fig. 9.20 Comparison of experimentally extracted, calculated and simulation threshold voltages.

Another source of error as pointed out above could be an increase in $\delta L$ with stress time, which will result in lower extracted ($\Delta N_{it}$) than that used in Fig. (9.20) and consequently lower extracted $V_t$. However within these limitations good overall agreement between measured and simulated threshold voltages validates the channel damage ($\Delta N_{it}$) extracted using the new extraction method. Further the agreement between simulated and calculated threshold voltages in Fig. 9.20 also supports the model for the threshold voltage presented in (9.41).

## 9.6 Generality of the New Methodology

The new method for $R_D$ extraction can in general be applied to any hot carrier stressed device and predicts consistent results in the long channel length limit, where conventional extraction procedures [9], [10], [12]-[14] are also applicable. In Figs. 9.21 and 9.22 the results of $R_D$ degradation using new and conventional method (using 9.6) are shown for 0.5μm and 1.5μm, 5V technologies respectively stressed under $I_{submax}$ condition. The comparison between the two methods in Figs. 9.21 and 9.22 helps to study the impact of scaling on the channel damage. In comparison to the totally decreasing extracted series resistance obtained using conventional methodologies for short channel devices reported in Chapter 7, it is seen that for longer channel lengths both the methods give approximately similar degradation behaviour

for short stress time. For longer stress time (>10s) the deviation in $R_D$ degradation using the two methods is more for the shorter of the two channel lengths.

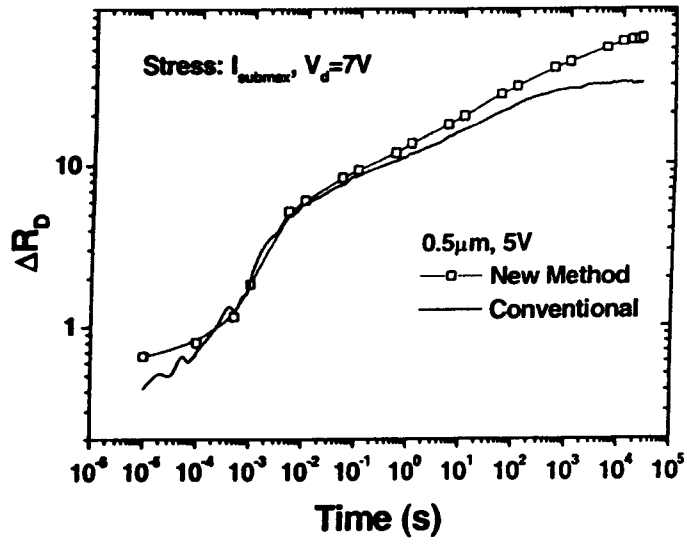


Fig. 9.21 Results of drain series resistance degradations obtained using new method (9.20) and conventional approach without modified universal mobility model for 0.5μm 5V technology, stressed at $I_{submax}$, $V_d$=7V.

This behaviour is consistent with the fact that as the channel length is increased, the peak electric field is reduced, causing lesser damage in the channel region. This leads to a lesser shift in universal model parameter $\theta_0 e^{-C\Delta Nit}$ in (9.20) from the corresponding unstressed values. For short stress time the amount of degradation in channel region is small as compared to spacer region because of the better gate oxide quality than the spacer oxide. Consequently, the deviation in universal model parameter of the damaged channel region is insignificant to affect $R_{SD}$ extraction.

As the stress time is increased, the larger damage in the channel region starts to affect the universal model behaviour. So for 0.5μm device in Fig. 9.21 because of its shorter channel length, the difference in $R_D$ degradation obtained using the two methods is more because of the greater channel damage. In contrast the longer channel device (1.5μm) in Fig. 9.22 shows a closer match in $R_D$ degradation obtained with the two methods.

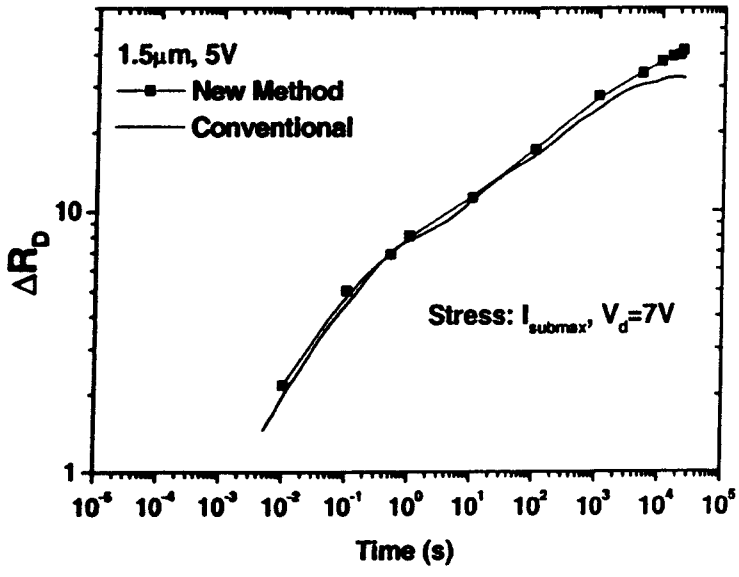


Fig. 9.22 Results of drain series resistance degradations obtained using new method (9.20) and conventional approach conventional approach without modified universal mobility model for 1.5μm, 5V technology, stressed at $I_{submax}$, $V_d$=7V.

## 9.7 Limitation of the New Methodology

Although the new method has been shown to successfully quantify the channel and spacer damages, the method does have its own limitation. The drawbacks associated with this method relate to the assumption made in considering the channel region as being uniformly damaged and the constancy of the extent of the channel damage with stress time. However, compared to the existing extraction methods discussed in Sec. 9.1, this limitation is only partial. Thus, the new methodology is a more accurate representation of the localised hot carrier damage and therefore, the extracted channel damage ($\Delta N_{it}$) is more realistic compared to the uniform damage assumed in existing methods, which will give lower extracted $\Delta N_{it}$ values. This is further supported by the results of Sec. 9.4.3 where good agreement between calculated (using channel damage obtained by new methodology) and measured threshold voltages.

The replacement of the localised damage by uniform equivalent damage will introduce error in the estimation of the channel charge and the resistance of the channel region. It is expected that the exact magnitude of the mobility degradation due to non-uniform damage will be different than that assumed for the uniformly damaged region. This can lead to errors in the extracted and true mobility degradation. Further the method is applicable under the

assumption that the extent (δL) of the damage in the channel region remains fixed after stress. However in reality small variations in δL after stress time is possible [17], [19]. But as demonstrated Sec. 9.3 this limitation only affects the extracted channel damage. Further, as seen in Table 9.3 the variation in δL does not significantly affect the extracted series resistance. Thus, despite these limitations, the method uniquely predicts the series resistance degradation behaviour.

## 9.8 Summary

In this Chapter, a new methodology for extraction of the series resistance and mobility degradation after hot carrier stress, applicable to a wide range of n-MOS technologies is presented. The methodology models the hot carrier stressed device as series combination of undamaged and damaged channel region, along with the series source drain resistance. While the on resistance model for undamaged channel remains unaltered, the resistance of damaged region is modelled by considering uniform damage of fixed extent, with interface charge dependent modified universal mobility model (presented in Chapter 8). The methodology successfully addressed the decreasing extracted series resistance problem encountered with conventional extraction methodology and gives a new insight into the hot carrier degradation behaviour of deep sub-micron technologies. The application of the new method to 2V and 3V technologies shows that series resistance degradation is an important factor in determining device degradation behaviour. Further, it is concluded that with scaling, major degradation to device performance is caused by channel damage and the resulting mobility degradation. The good correlation between the calculated and the measured parameters like $g_m$ and $V_t$ verifies the accuracy of the new method. The generality of the new method is demonstrated by the consistent degradation behaviour obtained for different technologies with wide-ranging channel lengths. Using the new method, the effect of device scaling on channel and spacer region damages can be studied. It is seen that in long channel limit, the parameter degradations extracted with new and conventional extraction methodologies give similar results. This consistency in extraction of parameter degradation behaviours further elucidates the generality of the new method.

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# CHAPTER 10

# CONCLUSIONS AND FUTURE WORK

In this Chapter the conclusions of this thesis are presented and some suggestions for future work are made.

This thesis studies the hot carrier degradation behaviour under different stress conditions in the range of deep submicron nMOS technologies designed for 5V, 3V and 2V operations. The work has three main objectives: 1) To study the degradation behaviour of these technologies under very short stress time scale, 2) To identify the roles of spacer and channel damages in the device degradation behaviour, 3) To study the mechanisms of spacer degradation, and 4) To develop a technique based on linear region characterisation enabling the roles of spacer and channel damages to be quantified through the series resistance and mobility degradation; and study the role of device scaling on the damage in channel and spacer regions.

## 10.1 Conclusions

(i) The hot carrier degradation of these technologies shows technology dependent two-stage degradation behaviour with early stage lasting up to 100ms. The degradation in the early stage is found to be maximum for 5V technology and successively decreases going down from 3V to 2V technologies. A model based on the series resistance degradation due to the damage in the spacer region in the early stage and the damage in the channel region in long term power law regime explains degradation behaviour well.

(ii) The analysis of the damage using series resistance and mobility degradation extraction methodology developed in Chapter 6 shows that for 5V technologies the damage in the early stage is dominated by the increase in the series resistance. Further it is found that the drain series resistance increase follows a two-stage evolution, which explains the observed early stage degradation behaviour for these technologies. In the long-term stress, the device degradation is controlled by the mobility degradation, while the series resistance degradation tends to saturate.

(iii) The charge pumping measurements can be used investigate the nature of the damage in the spacer region. For the studies carried on 5V technology, it is found that under $V_g \sim V_t$ and $I_{submax}$ conditions the damage is dominated by interface state generation. Under $V_g = V_d$ stress condition the damage to the spacer region is caused by combination of electron trapping and interface state generation.

(iv) The application of the conventional extraction methodology, used in the analysis of 5V technologies presented in Chapter 6, to the analysis of 3V and 2V technologies, gives decreasing extracted series resistance. This demonstrates the failure of the conventional extraction methodologies to quantify the degradation behaviour for the device technologies approaching quarter micron regime. It is concluded that as channel length is reduced and operating voltage decreased the damage in the channel region plays a more dominant role. For these technologies the greater damage in the channel region causes a significant change in the universal mobility behaviour, which is the underlying cause of the failure of the conventional parameter extraction methodology of Chapter 6. This leads to a need for modelling the effect of interface charge on the universal mobility model and for a new extraction methodology for parameter degradation after hot carrier stress.

(v) The effect of the interface charge in the channel region on the universal mobility behaviour can be studied using FN stress experiments. Because in this technique the carrier tunnelling across the gate oxide cause the damage, any damage in the spacer oxide and resulting series resistance degradation can be eliminated. It is shown using FN stress experiments that generation of the interface charge in the gate oxide causes the deviation in the universal mobility behaviour. This deviation in the universal behaviour can be attributed to the effect of partially screened coulomb scattering of the inversion layer carriers by generated interface charge. The resulting deviation in the universal behaviour can be empirically modelled as change in universal model parameters with interface charge. Using this approach, a modified universal mobility model is developed, which includes interface charge dependent universal model parameters to account for the observed deviation.

(vi) A generalised model of the hot carrier stressed device in the linear region operation can be represented as series combination of undamaged and damaged channel region.

While the mobility model for the unstressed channel region remains the same as that of the unstressed device, in the damaged channel the modified universal mobility model needs to be incorporated. This model forms the basis for a new extraction procedure presented in Chapter 9. This methodology overcomes the decreasing extracted series resistance problem associated with the conventional extraction procedure. The application of the new method to hot carrier stressed deep submicron technologies shows that series resistance degradation does play a role in determining the degradation behaviour. For 5V technologies, due to lower spacer doping and larger spread of electric field in the spacer region, there is greater damage in the spacer region and consequently more degradation in the series resistance is observed. For 3V and 2V technologies, higher LDD doping causes a lesser sensitivity of the damage in the spacer region to series resistance increase, and leads to a lower series resistance increase, despite the damage in the spacer region. The degradation for 2V and 3V technologies is much higher in the channel region, leading to the observation of mobility degradation at shorter time scales as well as higher long-term degradation.

## 10.2 Future Work

The study presented in this thesis leads into to new topics on which further research can be undertaken. Some of the important areas are:

(i) Nature of the Spacer Damage: using charge-pumping measurements the nature of the damage in the spacer region under different stress conditions for 5V technologies is studied. An independent study can be carried to verify the conclusions presented in this study using MOS devices fabricated using same materials and processes as that of the spacer deposition process in conventional CMOS technology. Further, as the charge pumping measurements to investigate the spacer damage has been done on 5V technologies, a similar work can to be carried out on 2V and 3V technologies.

(ii) The Modified Universal Mobility Model: The effect of oxide charge on the universal behaviour and dependence of model parameters on the oxide charge was studied. Although for the modelling purposes such a description is adequate, the modified universal model developed in this work is largely empirical. Further research can be undertaken to develop a model based on the detailed physical mechanisms responsible for the reported deviation behaviour. This could be achieved, for example, by

considering the effect of oxide charge on Coulomb scattering component of the universal mobility alone, incorporating screening that is responsible for the observed deviation behaviour.

(iii) Non-Uniform Channel Damage and its Stress Time Dependence: in the new extraction methodology for the series resistance and mobility degradation, the non-uniform damage in the channel region is treated as uniformly damaged region of fixed length. However, in practice, the precise damage profile is non-uniform, technology and stress condition dependent and can vary with the stress time. The methodology can be extended to incorporate a technology-dependent non-uniform damage profile, taking into account any variation of the extent of the damage with the stress time. This could be achieved by laterally profiled damage distribution as function of stress time by using charge-pumping measurements on single gate devices.

# LIST OF PUBLICATIONS


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